

SuZhou

CPU : Intel Arrandale
Chip Set : Intel Ibex Peak(PM55)
GFX : N11P / M-GE(40nm)
Remarks : Calpella Platform

Model Name : SuZhou-MH
PBA Name : MAIN
PCB Code : BA41-01190A
Dev. Step : PVR
Revision : 1.0
T.R. Date : 2009.11.3

Design	CHECK	APPROVAL
Xiaohong Zhang	Rujin Zheng	BC Lee

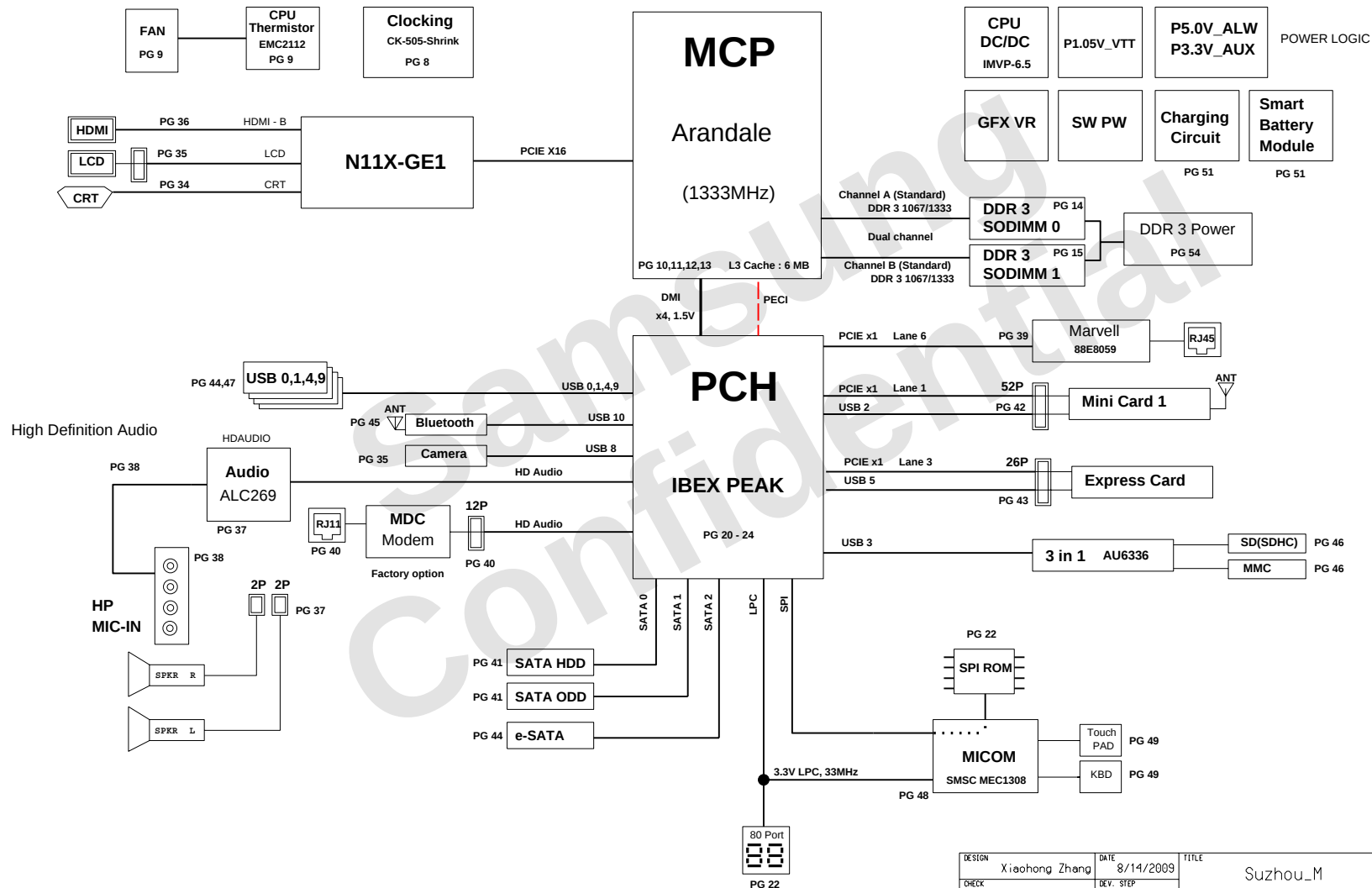
■ Owner : SEC Mobile R & D Signature : X

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DESIGN	Xiaohong Zhang	DATE	8/14/2009	TITLE	Suzhou_M	SAMSUNG
CHECK	Rujin Zheng	DEV. STEP	PV			ELECTRONICS
APPROVAL	BC LEE	REV	1.0			PART NO.
MODULE CODE		LAST EDIT	October 10, 2009 00:22:55 AM	PAGE	1 OF 62	BA41-01190/1/2A

BLOCK DIAGRAM



DESIGN	Xiaohong Zhang	DATE	8/14/2009	TITLE	Suzhou_M	SAMSUNG ELECTRONICS PART NO. BA41-01190/1/2A
CHECK	Rujin Zheng	DEV. STEP	PV		UNDEFINED	
APPROVAL	BC LEE	REV	1.0		UNDEFINED	
MODULE CODE		LAST EDIT	October 10, 2009 00:22:55 AM	PAGE	2 OF 62	

BOARD INFORMATION

SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

Voltage Rails	Active in
VDC P3.3V_MICOM P5.0V_ALW P5.0V_STB	Primary DC system power supply (7 to 21V) 3.3V always power rail (for Micom) 5.0V always power rail 5.0V always power rail
P5.0V_AUX P3.3V_AUX P1.5V_AUX	5.0V switched on power rail (off in S4-S5) 3.3V switched on power rail (off in S4-S5) 1.5V power rail for DDR (off in S4-S5)
P5.0V P3.3V P1.8V P1.5V P0.75V	5.0V switched power rail (off in S3-S5) 3.3V switched power rail (off in S3-S5) 1.8V switched power rail (off in S3-S5) 1.5V switched power rail (off in S3-S5) 0.9V power rail for DDR (off in S3-S5)
VCC_CORE EGFX_CORE P1.05V (VCCP) P1.1V_VTT	Core Voltage for CPU Core Voltage for GPU VCC for Clarkfield & IBEX Peak VTT for CLARDSFIELD & IBEX Peak

USB PORT Assign		PCI Express Assign	
PORT #	ASSIGNED TO	PORT #	ASSIGNED TO
0	SYSTEM PORT 0	1	Mini Card 1 (WLAN)
1	SYSTEM PORT 1	2	NC
2	Mini PCI Express 1	3	EXPRESS CARD
3	NC	4	NC
4	SYSTEM PORT 4	5	NC
5	EXPRESS CARD	6	NC
6	NC (N/A WITH HM55)	7	NC (N/A WITH HM55)
7	NC (N/A WITH HM55)	8	NC (N/A WITH HM55)
8	Multi Memory Card Controller		
9	SYSTEM PORT 9		
10	Bluetooth		
11	Camera		
12	NC		
13	NC		

SATA PORT Assign	
PORT #	ASSIGNED TO
0	HDD
1	ODD
2	(N/A WITH HM55)
3	(N/A WITH HM55)
4	e-SATA

Crystal / Oscillator

TYPE	FREQUENCY	DEVICE	USAGE
Crystal	32.768KHz	IBEX-PEAK	Real Time Clock
Crystal	10MHz	MICOM	HD64F2169/2160
Crystal	14.318MHz	CLOCK-Generator	CK-505
Crystal	25MHz	LAN	Intel LAN
Crystal	25MHz	IBEX PEAK	

LCD Pannel Detect (TBD)

Devices	Resolution	PANNEL_DETECT_0
---------	------------	-----------------

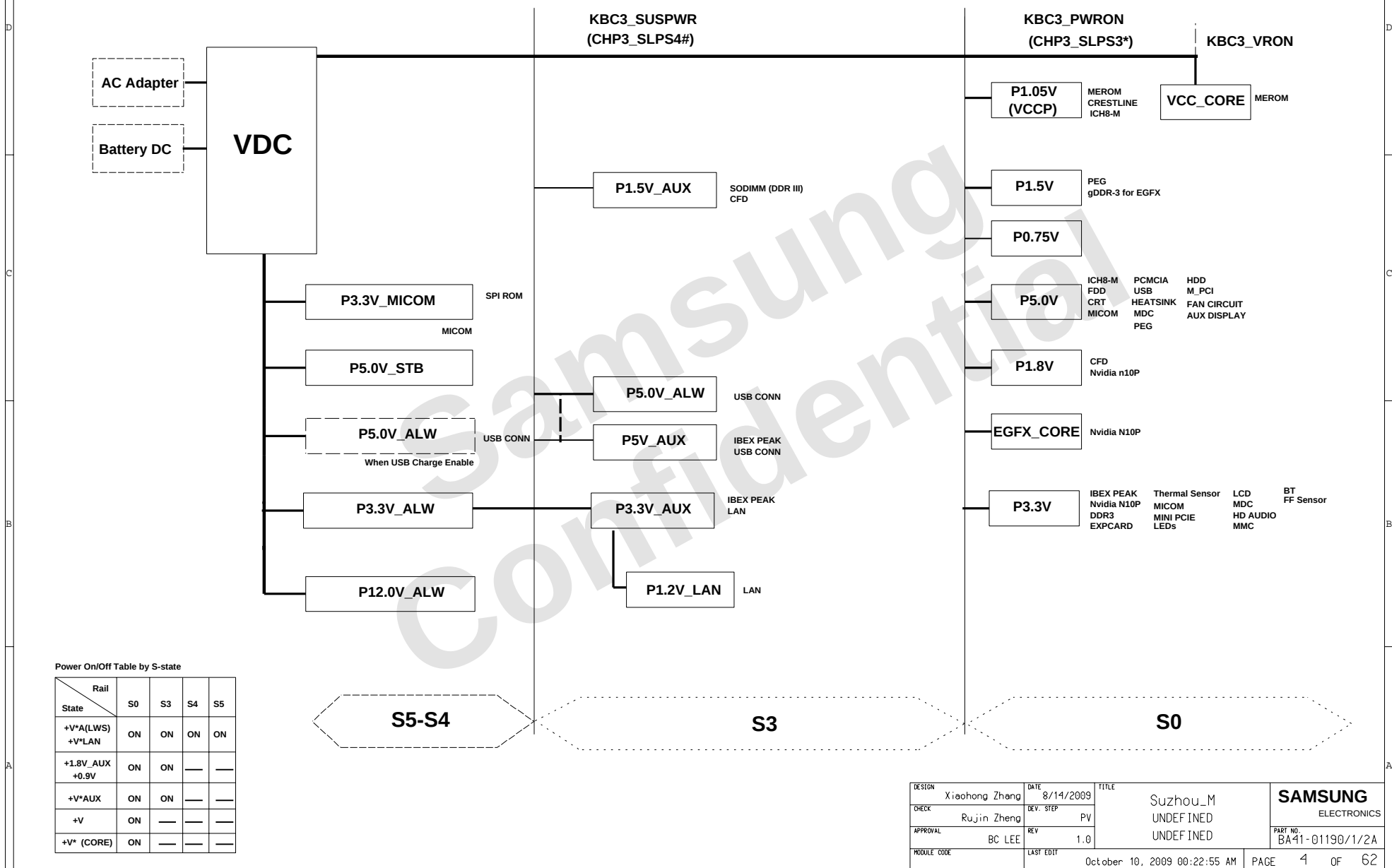
I²C / SMB Address

Devices	Address	Hex	Bus
IBEX PEAK	Master	-	SMBUS Master
CPU Thermal Sensor	0111 101x	7Ah	Thermal Sensor
SODIMM0	1010 000x	A0h	-
SODIMM1	1010 010x	A4h	-
Thermal Sensor on SODIMM0	0011 000x	30h	-
Thermal Sensor on SODIMM1	0011 010x	34h	-
CK-505M Shrink(Clock Generator)	1101 001x	D2h	Clock, Unused Clock Output Disable
Thermal Sensor on board	1101 100x	98h	
Power thermal management TS	1101 011x	96h	

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APPROVAL	BC LEE	REV	1.0		UNDEFINED	
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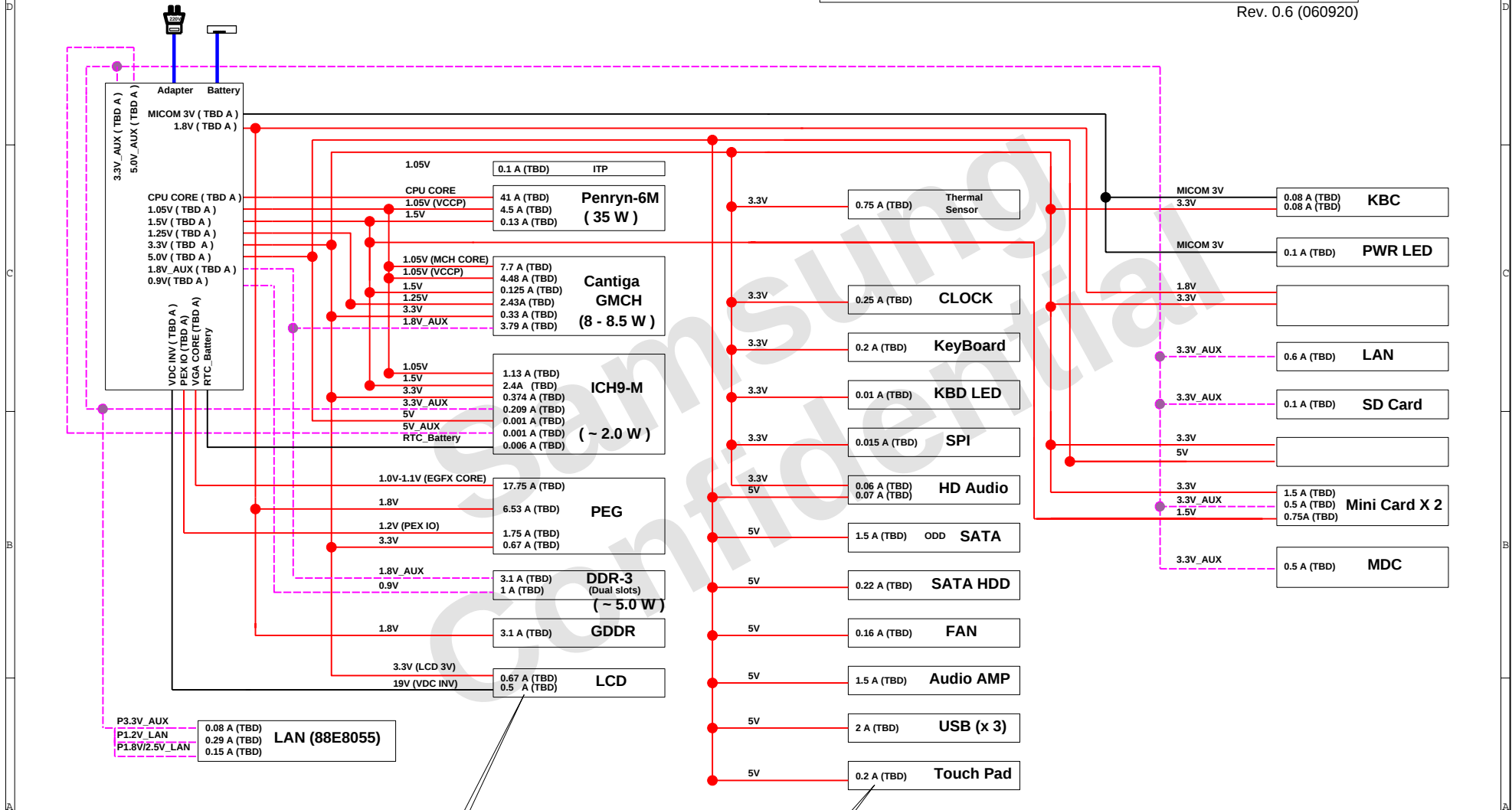
POWER DIAGRAM

Rev 0.1



POWER RAILS ANALYSIS

Rev. 0.6 (060920)

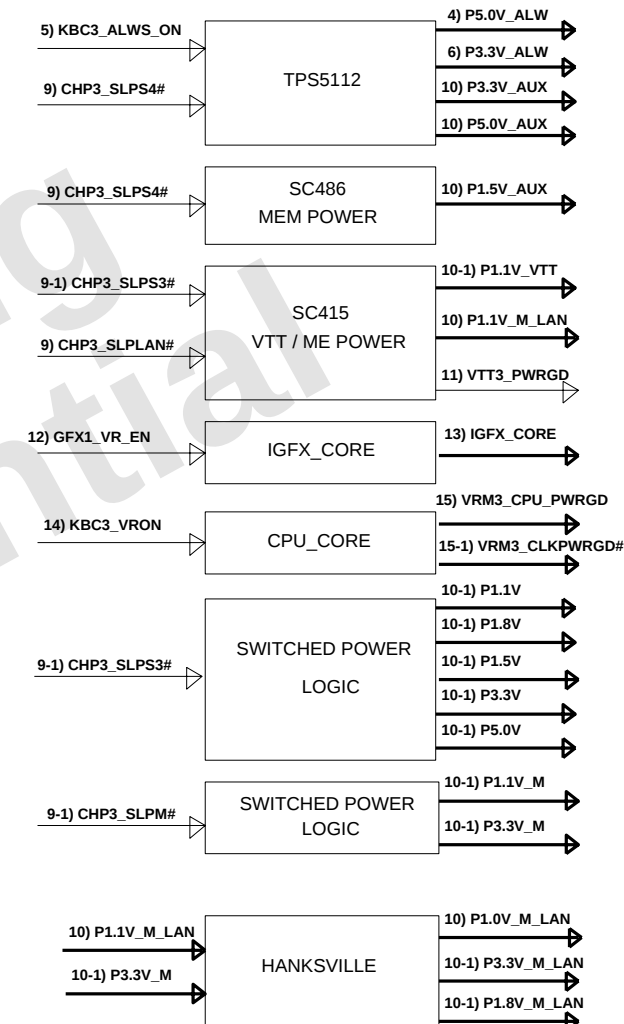
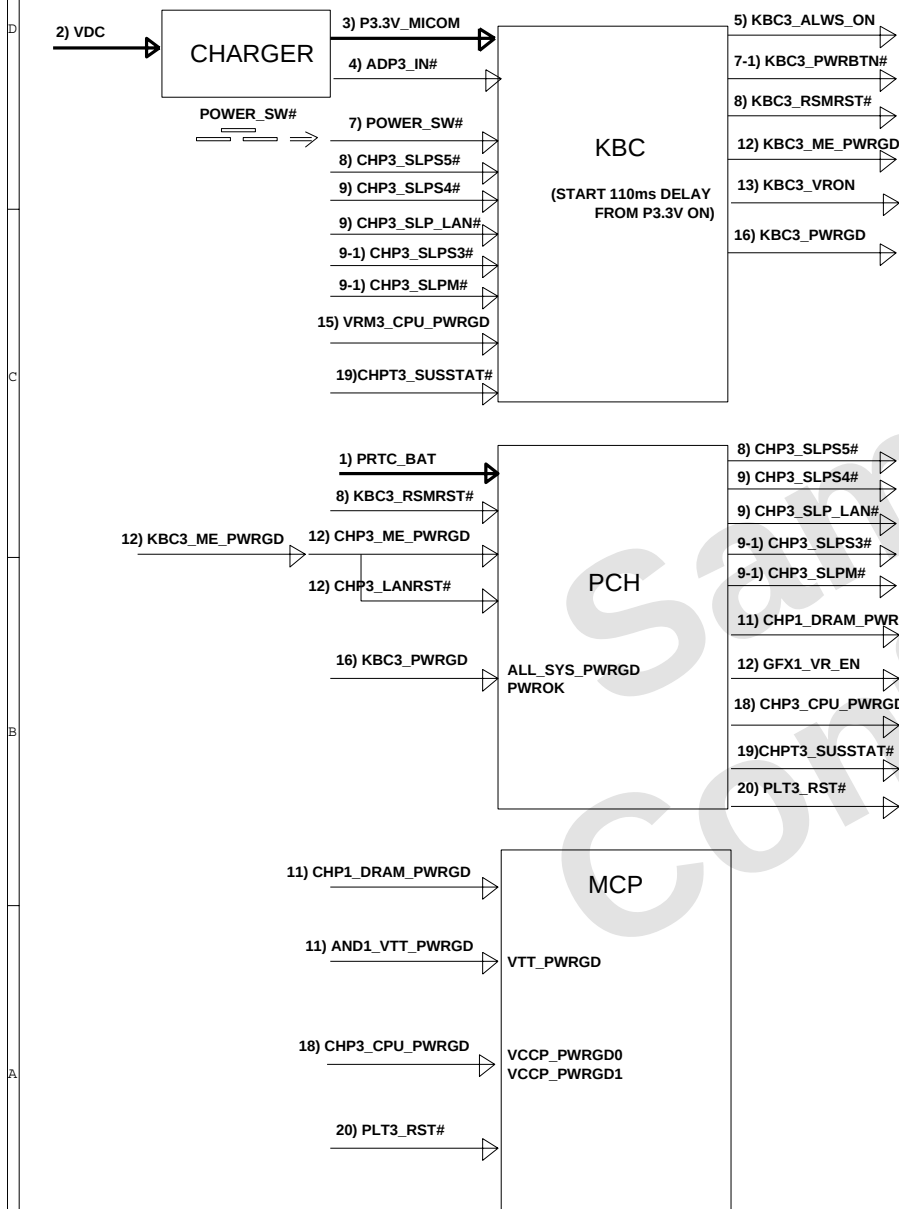


Value by Datasheet/Application notes (Value by measurement)

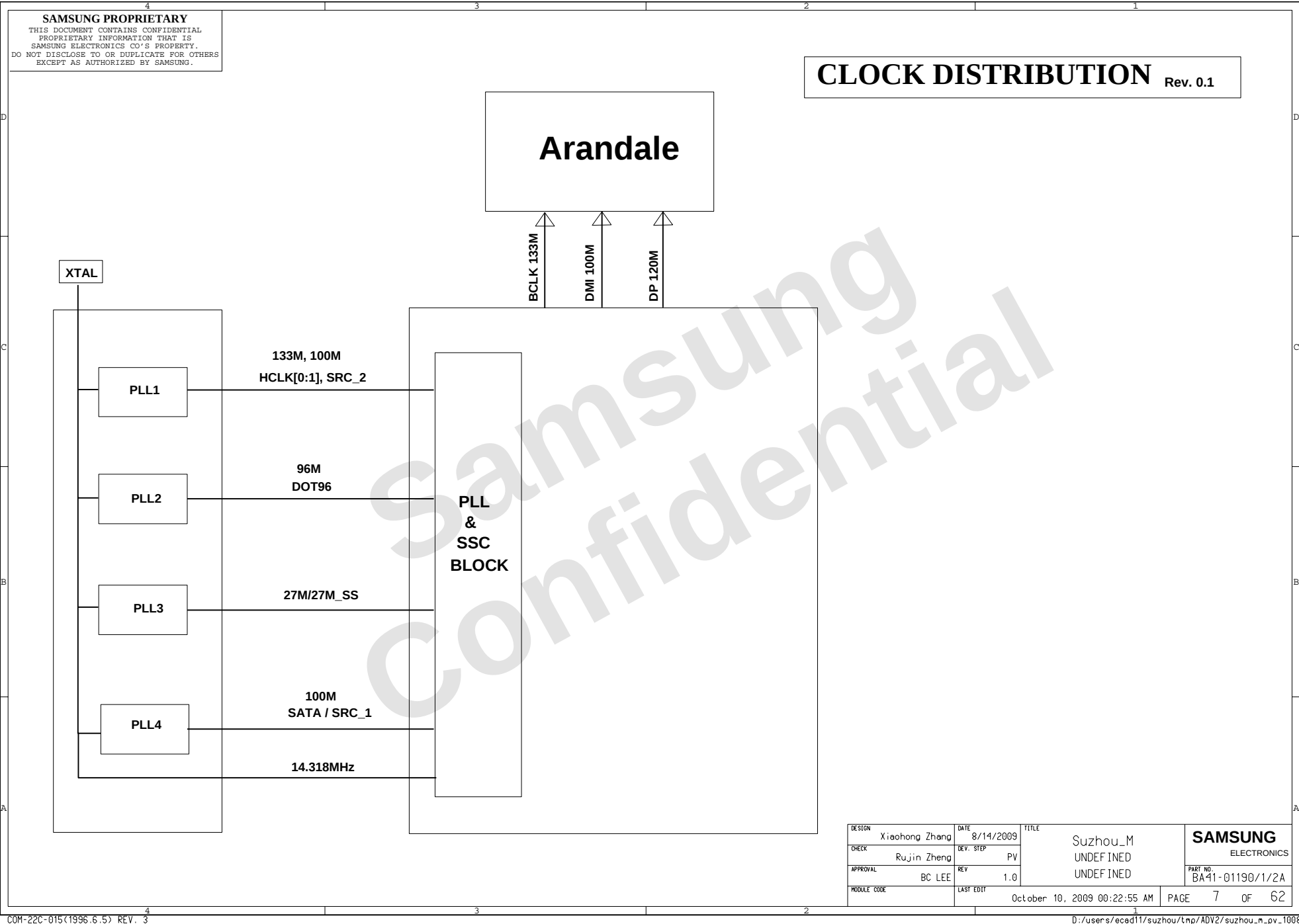
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PRELIMINARY

POWER SEQUENCE Rev. 0.5



DESIGN	Xiaohong Zhang	DATE	8/14/2009	TITLE	Suzhou_M	SAMSUNG ELECTRONICS
CHECK	Rujin Zheng	DEV. STEP	PV		UNDEFINED	
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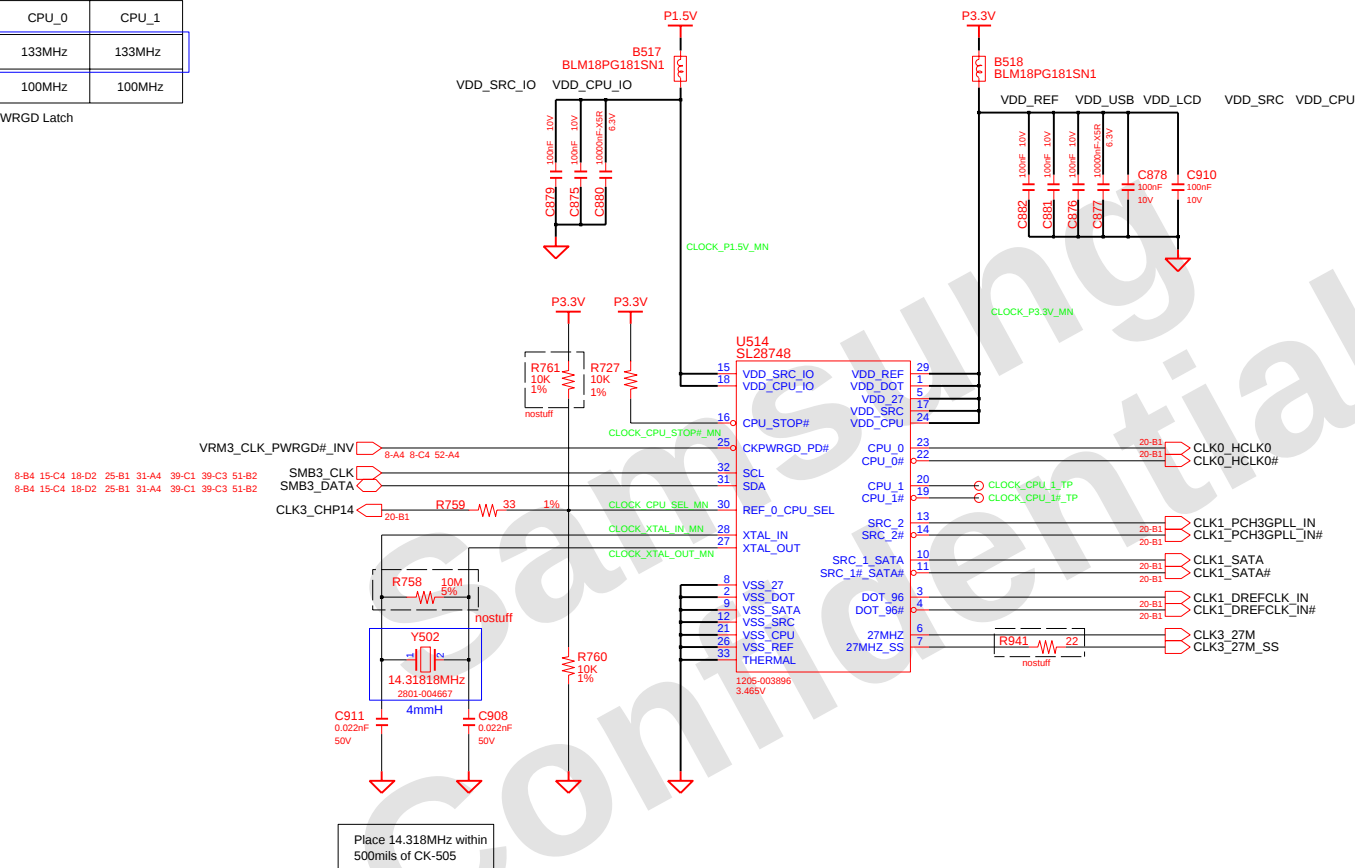
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CK505M SHRINK VERSION

CPU_MODE SEL

Pin 30	CPU_0	CPU_1
CPU_SEL = 0	133MHz	133MHz
CPU_SEL = 1	100MHz	100MHz

*CPU_SEL During CK_PWRGD Latch



DRAW	Xiaohong Zhang	DATE	8/12/2006	TITLE	Suzhou_M	SAMSUNG ELECTRONICS PART NO. BA41-01190/1/2A
CHECK	Rujin Zheng	DEV. STEP	PV		Main_Clock_Circuit	
APPROVAL	BC LEE	REV	1.0		CK-Clock_505M	
MODULE CODE	undefined	LAST EDIT	October 10, 2009 00:22:55 AM	PAGE	8 OF 62	

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THERMAL SENSOR & FAN CONTROL

ADDRESSSEL MODE

0	0101 111xb
✓ HIGH Z	0111 101xb (7A)
1	0101 110xb

SHDNSEL MODE

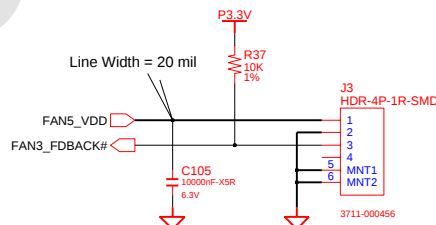
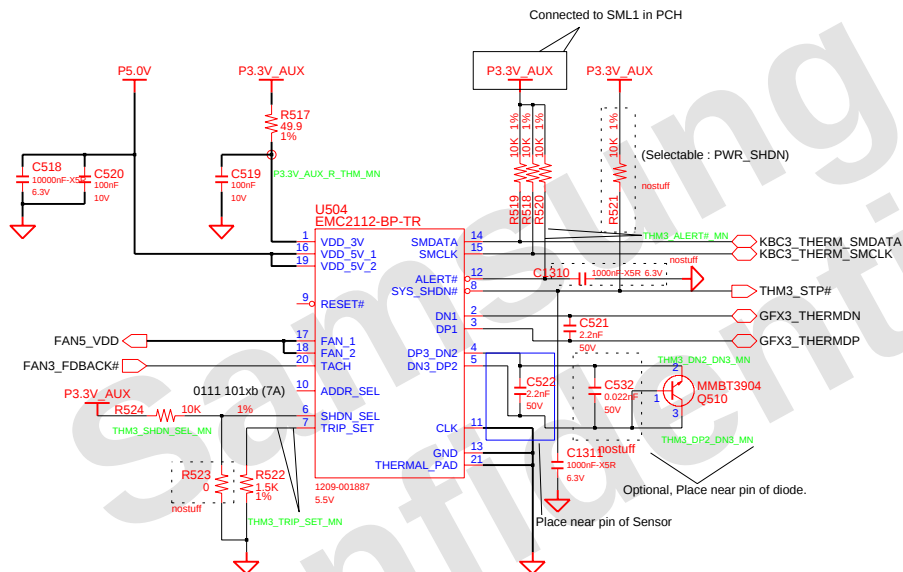
0	INTEL TR MODE
✓ HIGH Z	AMD CPU/DIODE MODE
1	EXT.DIODE 2 MODE

TRIP_SET Resistor Setting (60 ~ 122 C)

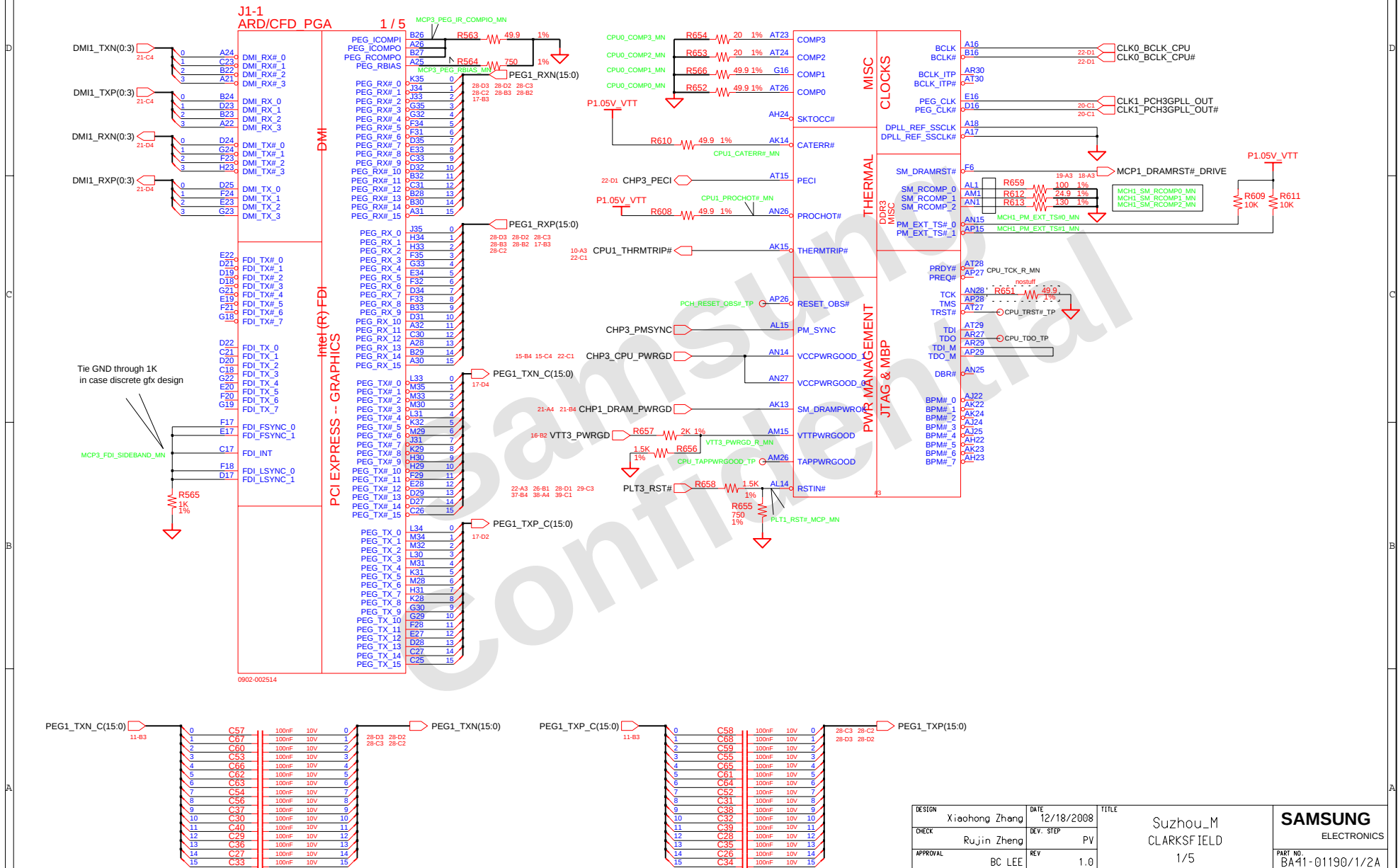
60	0.0
95	1500
96	1580
97	1690
98	1820
99	1960
100	2050
101	2210
102	2370
✓ 103	2550
104	2740
105	2940
122	49900

$$V_{Trip} = (T_{Trip} - T_{Min}) / 80$$

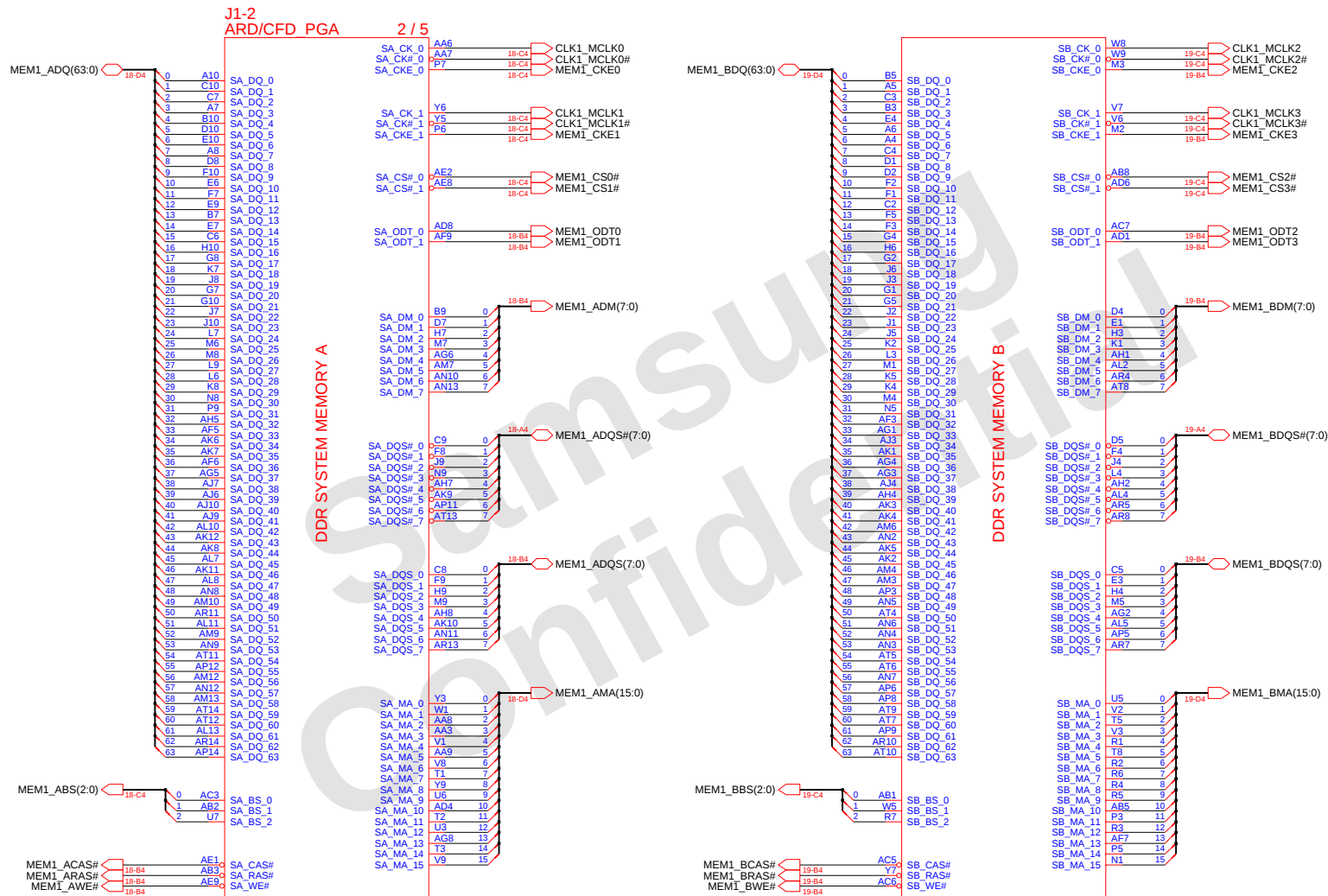
V_{Trip} : TRIP_SET Voltage
 T_{Min} : Minimum Temperature



ARRANDALE PROCESSOR (DMI,PEG, FDI)



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APPROVAL	BC LEE	REV	1.0			
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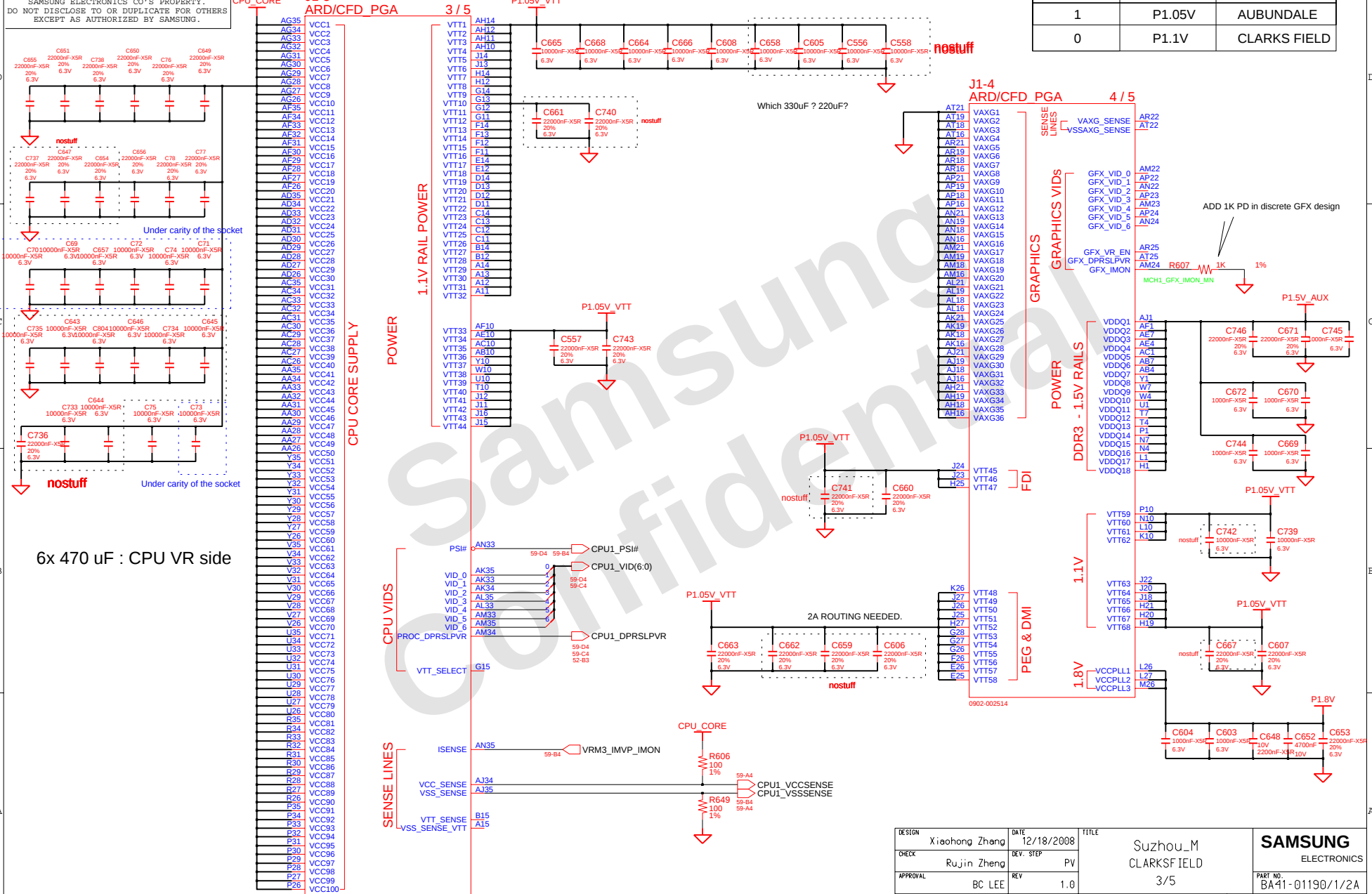
0902-002514

DESIGN	Xiaohong Zhang	DATE	12/18/2008	TITLE Suzhou_M CLARKSFIELD 2/5		SAMSUNG ELECTRONICS PART NO. BA41-01190/1/2A	
CHECK	Rujin Zheng	DEV. STEP	PV				
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ALL VTT DECAP IS SHARED(10uFX9, 22uFx7)

VTT_SEL	VOLTAGE	CPU
1	P1.05V	AUBUNDALE
0	P1.1V	CLARKS FIELD



DESIGN	Xiaohong Zhang	DATE	12/18/2008	TITLE	Suzhou_M CLARKSFIELD 3/5	SAMSUNG ELECTRONICS PART NO. BA41-01190/1/2A
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J1-5
ARD/CFD_PG#5 / 5

VSS#120	VSS1	VSS81	AE34
AR17	VSS2	VSS82	AE35
AR31	VSS3	VSS83	AE36
AR28	VSS4	VSS84	AE37
AR26	VSS5	VSS85	AE38
AR24	VSS6	VSS86	AE39
AR23	VSS7	VSS87	AE40
AR20	VSS8	VSS88	AE41
AR17	VSS9	VSS89	AE42
AR15	VSS10	VSS90	AE43
AR12	VSS11	VSS91	AE44
AR9	VSS12	VSS92	AE45
AR6	VSS13	VSS93	AE46
AR3	VSS14	VSS94	AE47
AP20	VSS15	VSS95	AE48
AP17	VSS16	VSS96	AE49
AP13	VSS17	VSS97	AE50
AP10	VSS18	VSS98	AE51
AP7	VSS19	VSS99	AE52
AP4	VSS20	VSS100	AE53
AN32	VSS21	VSS101	AE54
AN34	VSS22	VSS102	AE55
AN31	VSS23	VSS103	AE56
AN23	VSS24	VSS104	AE57
AN20	VSS25	VSS105	AE58
AN17	VSS26	VSS106	AE59
AM29	VSS27	VSS107	AE60
AM27	VSS28	VSS108	AE61
AM25	VSS29	VSS109	AE62
AM20	VSS30	VSS110	AE63
AM17	VSS31	VSS111	AE64
AM14	VSS32	VSS112	AE65
AM11	VSS33	VSS113	AE66
AM8	VSS34	VSS114	AE67
AM5	VSS35	VSS115	AE68
AM2	VSS36	VSS116	AE69
AL34	VSS37	VSS117	AE70
AL31	VSS38	VSS118	AE71
AL23	VSS39	VSS119	AE72
AL20	VSS40	VSS120	AE73
AL17	VSS41	VSS121	AE74
AL12	VSS42	VSS122	AE75
AL9	VSS43	VSS123	AE76
AL6	VSS44	VSS124	AE77
AL3	VSS45	VSS125	AE78
AK29	VSS46	VSS126	AE79
AK27	VSS47	VSS127	AE80
AK25	VSS48	VSS128	AE81
AK20	VSS49	VSS129	AE82
AK17	VSS50	VSS130	AE83
AK13	VSS51	VSS131	AE84
AK9	VSS52	VSS132	AE85
AK6	VSS53	VSS133	AE86
AK3	VSS54	VSS134	AE87
AJ14	VSS55	VSS135	AE88
AJ11	VSS56	VSS136	AE89
AJ8	VSS57	VSS137	AE90
AJ5	VSS58	VSS138	AE91
AJ2	VSS59	VSS139	AE92
AH35	VSS60	VSS140	AE93
AH34	VSS61	VSS141	AE94
AH33	VSS62	VSS142	AE95
AH32	VSS63	VSS143	AE96
AH31	VSS64	VSS144	AE97
AH30	VSS65	VSS145	AE98
AH29	VSS66	VSS146	AE99
AH28	VSS67	VSS147	AE100
AH27	VSS68	VSS148	AE101
AH26	VSS69	VSS149	AE102
AH20	VSS70	VSS150	AE103
AH17	VSS71	VSS151	AE104
AH13	VSS72	VSS152	AE105
AH9	VSS73	VSS153	AE106
AH6	VSS74	VSS154	AE107
AH3	VSS75	VSS155	AE108
AG10	VSS76	VSS156	AE109
AF8	VSS77	VSS157	AE110
AF4	VSS78	VSS158	AE111
AF2	VSS79	VSS159	AE112
AC35	VSS80	VSS160	AE113

0002-002514

K27	VSS161
K9	VSS162
K6	VSS163
K3	VSS164
J32	VSS165
J30	VSS166
J21	VSS167
J19	VSS168
H35	VSS169
H32	VSS170
H26	VSS171
H22	VSS172
H19	VSS173
H15	VSS174
H13	VSS175
H11	VSS176
H8	VSS177
H5	VSS178
H2	VSS179
G34	VSS180
G31	VSS181
G20	VSS182
G9	VSS183
G6	VSS184
G3	VSS185
F30	VSS186
F27	VSS187
F25	VSS188
F22	VSS189
F19	VSS190
F16	VSS191
F13	VSS192
F10	VSS193
F7	VSS194
F4	VSS195
E29	VSS196
E24	VSS197
E21	VSS198
E18	VSS199
E13	VSS200
E11	VSS201
E8	VSS202
E5	VSS203
E2	VSS204
D33	VSS205
D30	VSS206
D26	VSS207
D23	VSS208
D20	VSS209
D17	VSS210
D13	VSS211
D9	VSS212
D6	VSS213
D3	VSS214
C34	VSS215
C32	VSS216
C29	VSS217
C26	VSS218
C22	VSS219
C20	VSS220
C19	VSS221
C16	VSS222
C13	VSS223
B31	VSS224
B25	VSS225
B21	VSS226
B18	VSS227
B17	VSS228
B13	VSS229
B11	VSS230
B8	VSS231
B6	VSS232
B4	VSS233
A29	VSS234
A27	VSS235
A23	VSS236
A20	VSS237
A9	VSS238

VSS

NCTF

AT35	VSS_NCTF1
AT1	VSS_NCTF2
AR34	VSS_NCTF3
B34	VSS_NCTF4
B2	VSS_NCTF5
B1	VSS_NCTF6
A35	VSS_NCTF7

CPU_VSS_NCTF3
CPU_VSS_NCTF4
CPU_VSS_NCTF5

R650

3.01K 1%

CPU_CFG_7_R_MN

CPU_RSVD17_TP

CPU_RSVD18_TP

AP25

AL25

AL24

AL22

AJ33

AG9

M27

L25

J17

H17

G25

C17

E31

E30

AM30

AM28

AP31

AL32

AL30

AM31

AM29

AM32

AK32

AK31

AK28

AJ28

AK30

AK32

AJ32

AJ28

CFG 15

CFG 16

CFG 17

RSVD_TP_86

B19

A18

RSVD15

RSVD16

RSVD17

RSVD18

U9

RSVD19

T9

RSVD20

RSVD21

RSVD22

AC9

AB9

RSVD23

RSVD24

RSVD25

RSVD26

RSVD27

RSVD28

RSVD29

RSVD30

RSVD31

RSVD32

RSVD33

RSVD34

RSVD35

RSVD36

RSVD37

RSVD38

RSVD39

(VSS) RSVD86

RSVD86

RSVD87

RSVD88

RSVD89

RSVD90

RSVD91

RSVD92

RSVD93

RSVD94

RSVD95

RSVD96

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RSVD103

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RSVD154

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RSVD159

RSVD160

RSVD161

RSVD162

RSVD163

RSVD164

RSVD165

RSVD166

RSVD167

RSVD168

RSVD169

RSVD170

RSVD171

RSVD172

RSVD173

RSVD174

RSVD175

RSVD176

RSVD177

RSVD178

RSVD179

RSVD180

RSVD181

RSVD182

RSVD183

RSVD184

RSVD185

RSVD186

RSVD187

RSVD188

RSVD189

RSVD190

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RSVD196

RSVD197

RSVD198

RSVD199

RSVD200

RSVD201

RSVD202

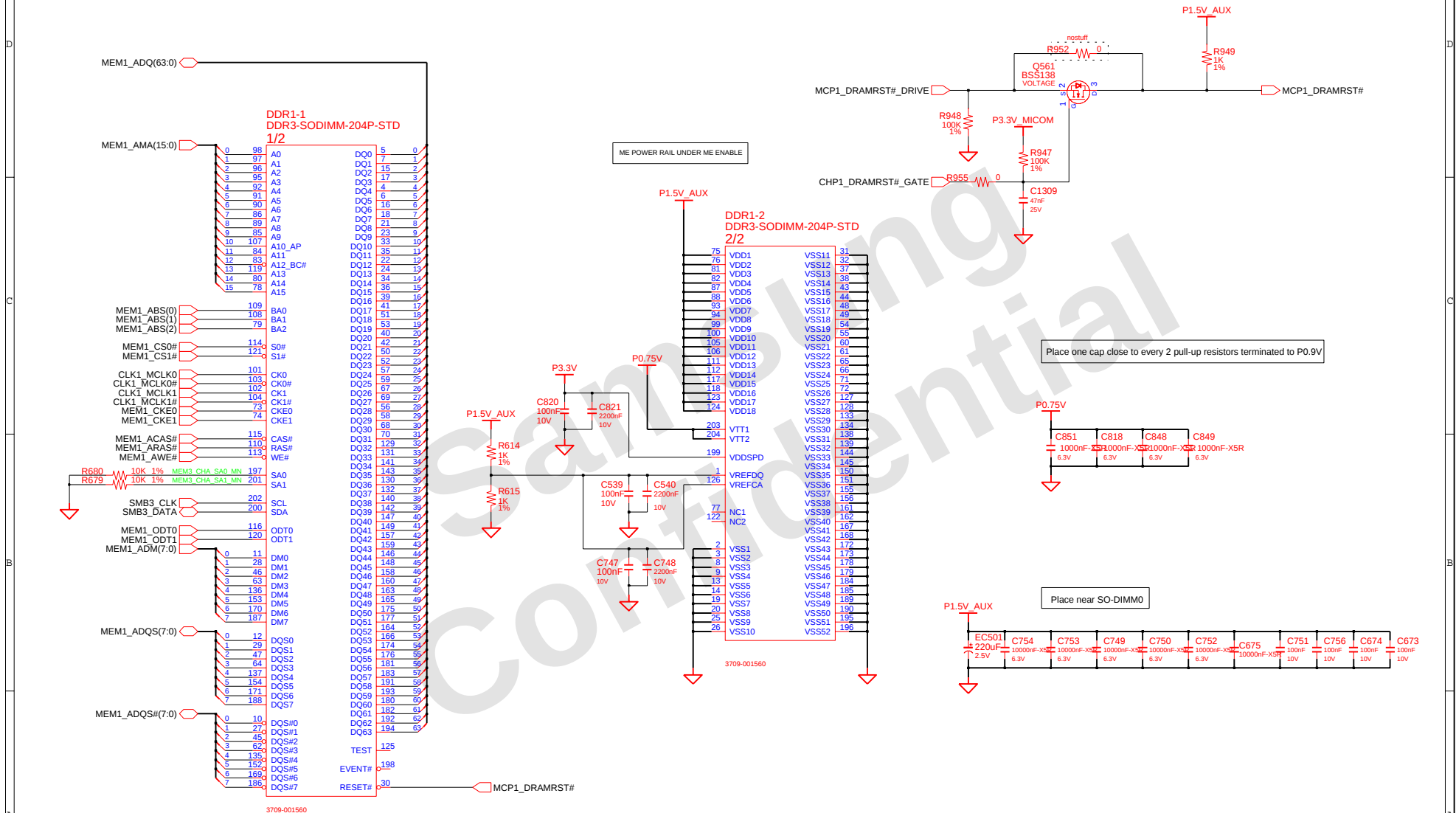
RSVD203

RSVD204

RSVD205

DDR SO-DIMM #0

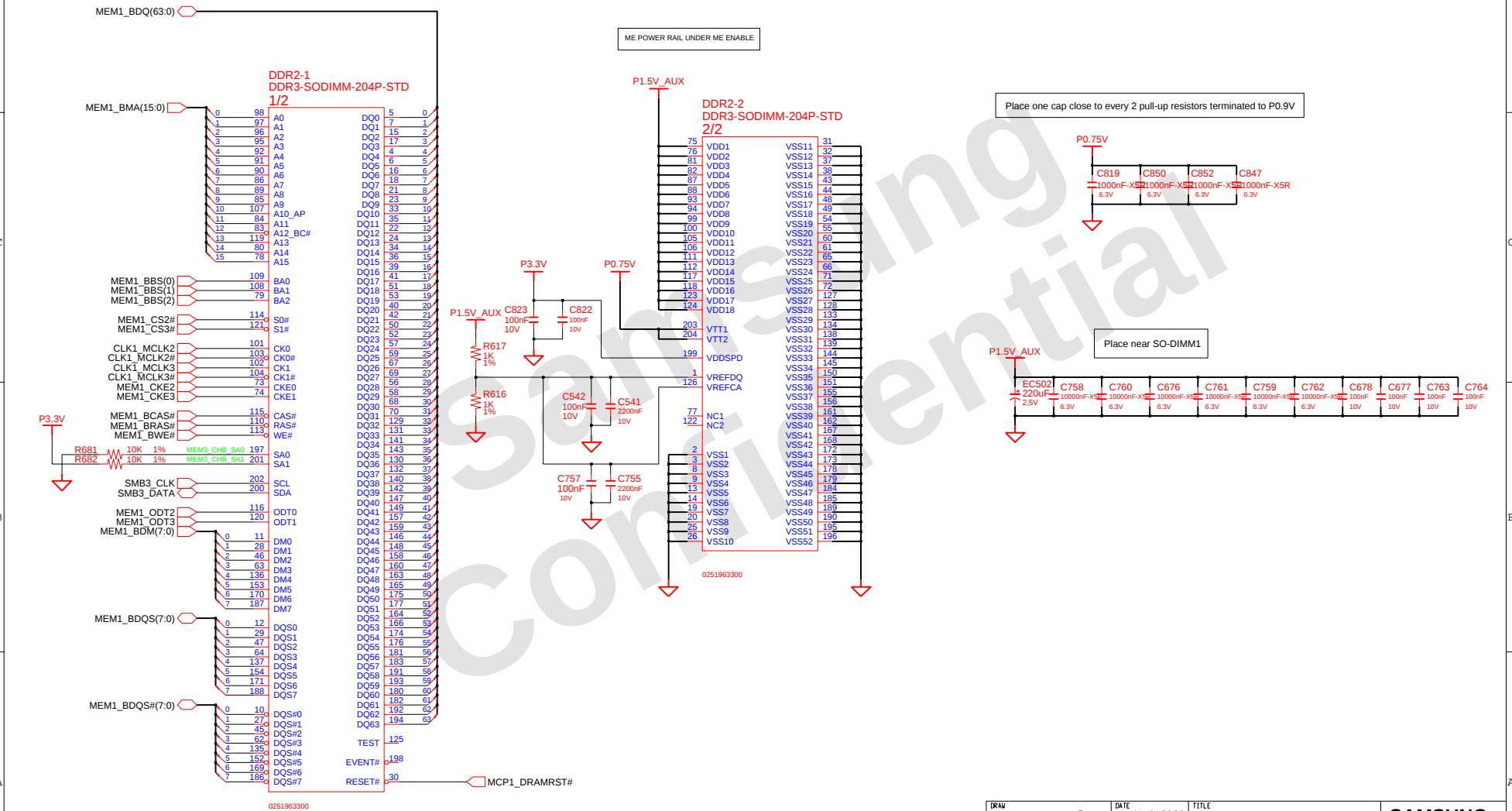
Height : 5.2mm (Reverse)



DRAW	Xiaohong Zhang	DATE	11/8/2006	TITLE	Suzhou_M SODIMM_REV DDR3 CH A	SAMSUNG ELECTRONICS PART NO. BA41-01190/1/2A
CHECK	Rujin Zheng	DEV. STEP	PV			
APPROVAL	BC LEE	REV	1.0			
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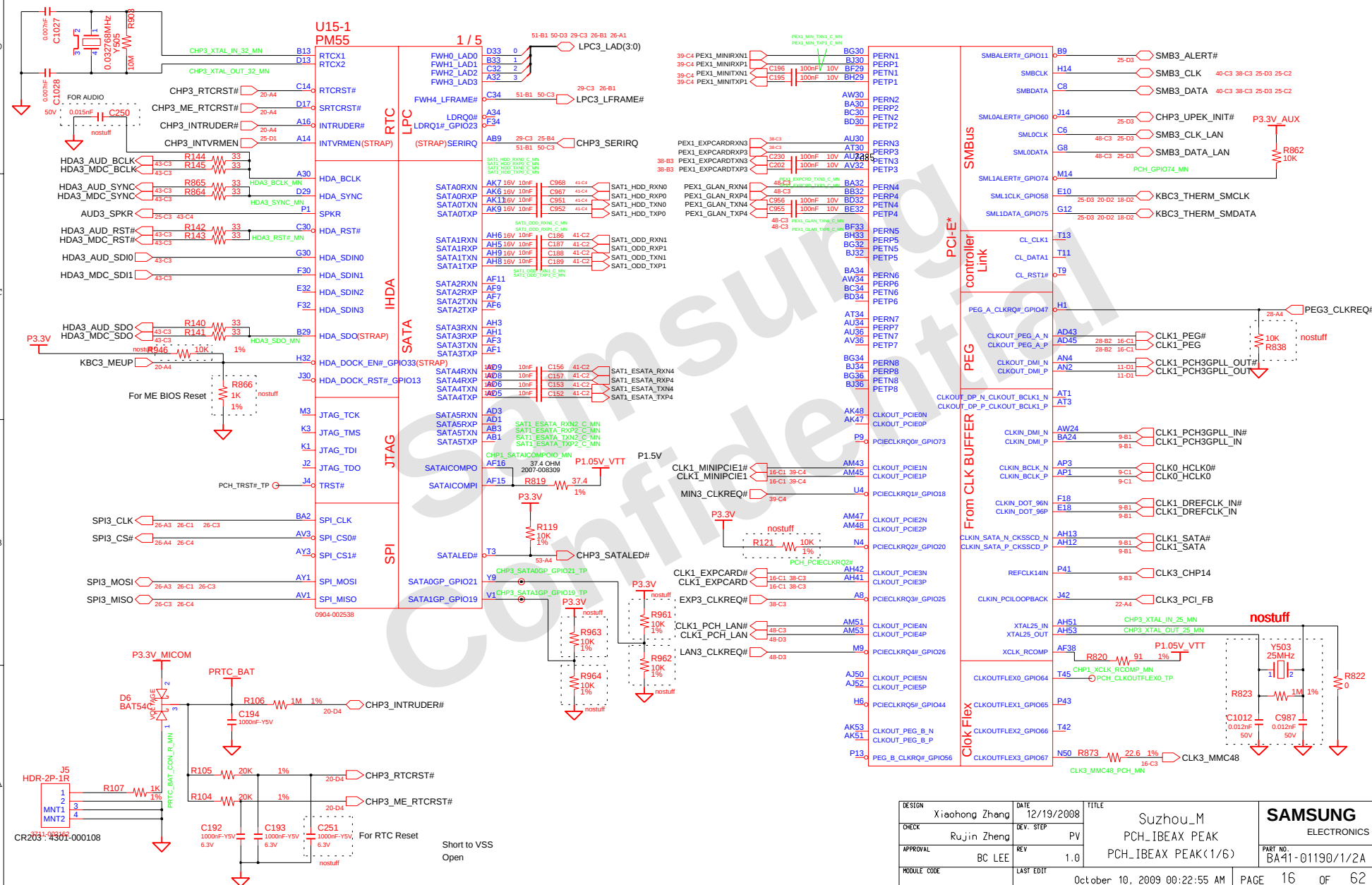
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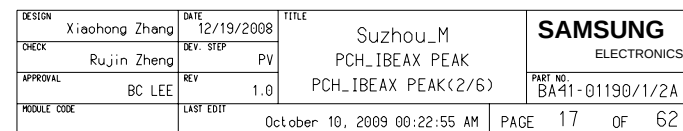
Height : 9.2mm (Reverse)

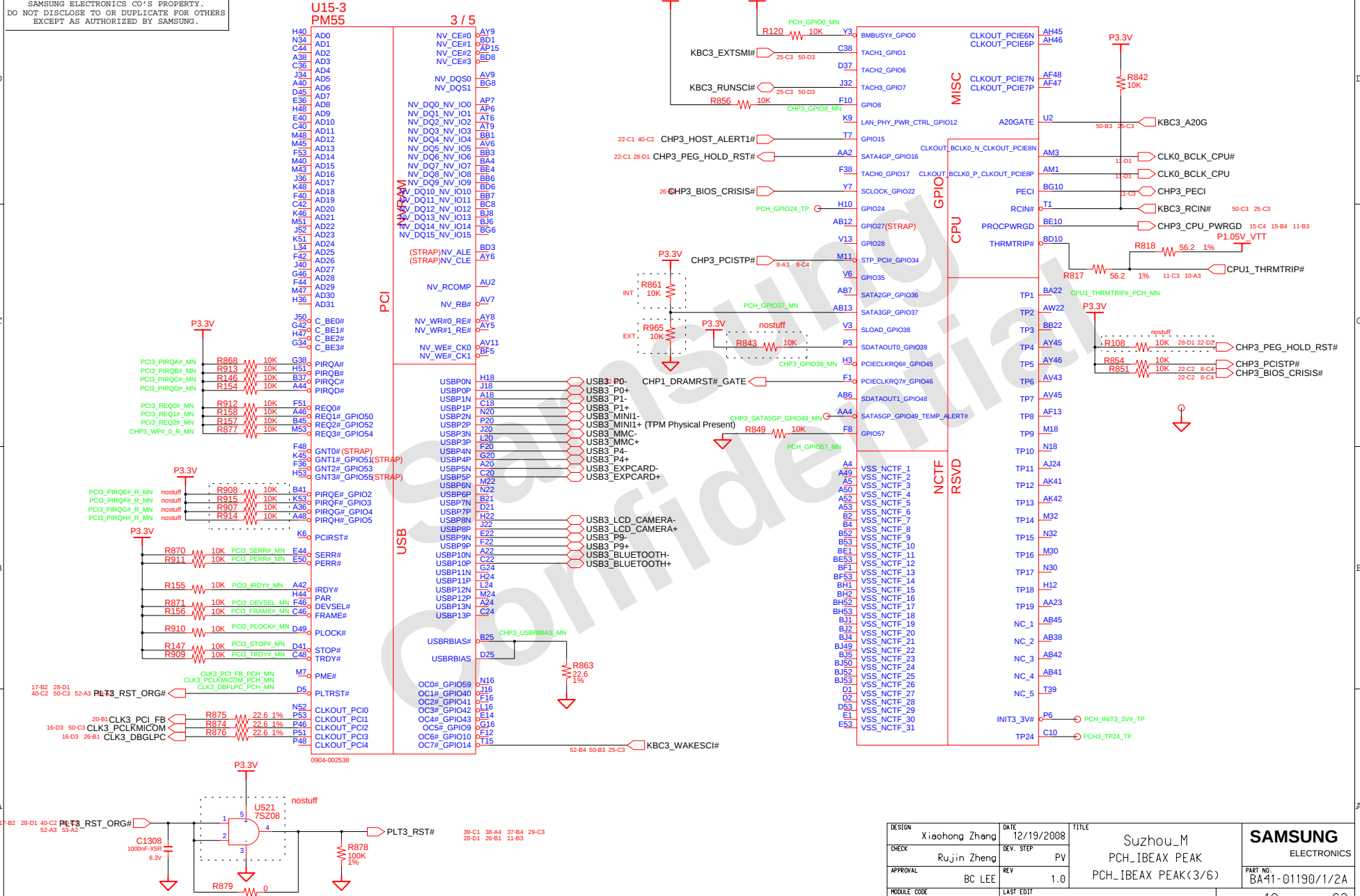


DRAW	Xiaohong Zhang	DATE	11/8/2006	TITLE	Suzhou_M SODIMM_REV DDR3 CH B	SAMSUNG ELECTRONICS PART NO. BA41-01190/1/2A
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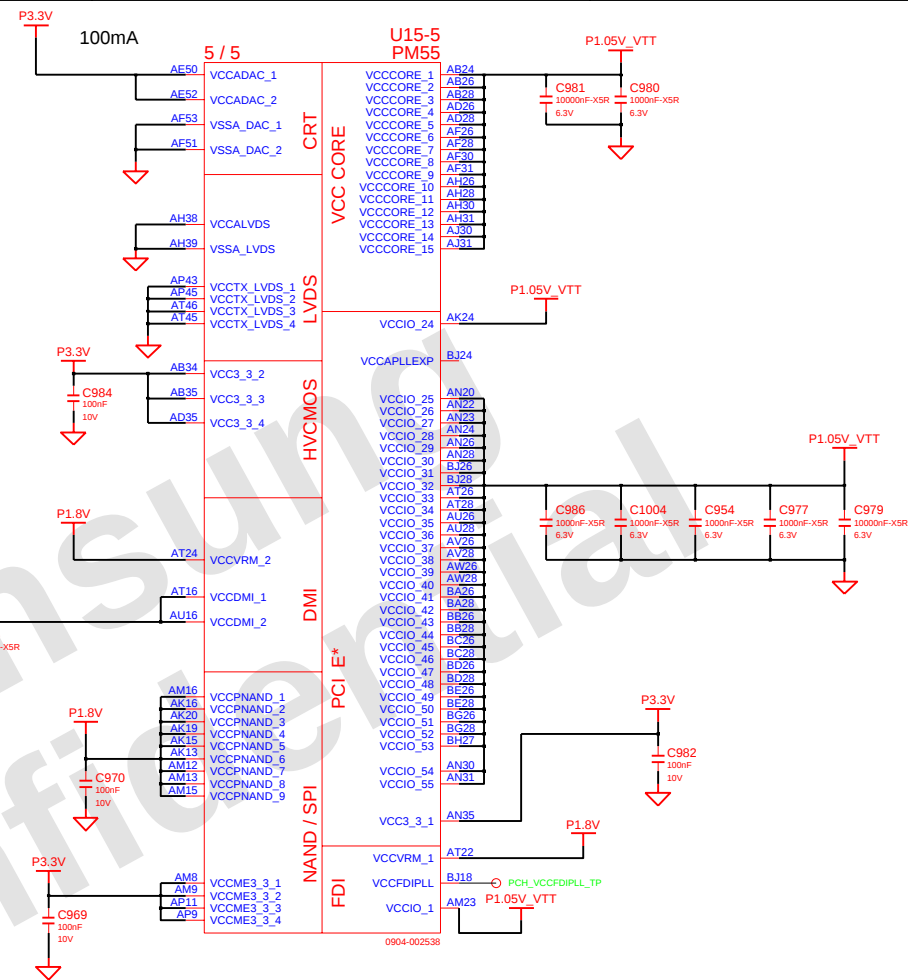
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COM-22C-015(1996.6.5) REV. 3

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H49	VSS_259	VSS_159	AY7
H5	VSS_260	VSS_160	B11
J24	VSS_261	VSS_161	B15
K11	VSS_262	VSS_162	B19
K43	VSS_263	VSS_163	B23
K7	VSS_264	VSS_164	B31
L14	VSS_265	VSS_165	B35
L18	VSS_266	VSS_166	B39
L2	VSS_267	VSS_167	B43
L22	VSS_268	VSS_168	B47
L32	VSS_269	VSS_169	B7
L36	VSS_270	VSS_170	BC12
L40	VSS_271	VSS_171	BB12
L52	VSS_272	VSS_172	BB16
M12	VSS_273	VSS_173	BB20
M16	VSS_274	VSS_174	BB24
M20	VSS_275	VSS_175	BB30
M38	VSS_276	VSS_176	BB34
M42	VSS_277	VSS_177	BB38
M46	VSS_278	VSS_178	BB42
M49	VSS_279	VSS_179	BB46
M5	VSS_280	VSS_180	BB5
M8	VSS_281	VSS_181	BC10
N24	VSS_282	VSS_182	BC14
N28	VSS_283	VSS_183	BC18
N32	VSS_284	VSS_184	BC2
N36	VSS_285	VSS_185	BC22
N40	VSS_286	VSS_186	BC26
N44	VSS_287	VSS_187	BC30
N48	VSS_288	VSS_188	BC34
N52	VSS_289	VSS_189	BC38
N56	VSS_290	VSS_190	BC42
N60	VSS_291	VSS_191	BC46
N64	VSS_292	VSS_192	BC50
N68	VSS_293	VSS_193	BD0
N72	VSS_294	VSS_194	BD04
N76	VSS_295	VSS_195	BD08
N80	VSS_296	VSS_196	BD12
N84	VSS_297	VSS_197	BD16
N88	VSS_298	VSS_198	BD20
N92	VSS_299	VSS_199	BD24
N96	VSS_300	VSS_200	BD28
N100	VSS_301	VSS_201	BD32
N104	VSS_302	VSS_202	BD36
N108	VSS_303	VSS_203	BD40
N112	VSS_304	VSS_204	BD44
N116	VSS_305	VSS_205	BD48
N120	VSS_306	VSS_206	BD52
N124	VSS_307	VSS_207	BD56
N128	VSS_308	VSS_208	BD60
N132	VSS_309	VSS_209	BD64
N136	VSS_310	VSS_210	BD68
N140	VSS_311	VSS_211	BD72
N144	VSS_312	VSS_212	BD76
N148	VSS_313	VSS_213	BD80
N152	VSS_314	VSS_214	BD84
N156	VSS_315	VSS_215	BD88
N160	VSS_316	VSS_216	BD92
N164	VSS_317	VSS_217	BD96
N168	VSS_318	VSS_218	BD100
N172	VSS_319	VSS_219	BD104
N176	VSS_320	VSS_220	BD108
N180	VSS_321	VSS_221	BD112
N184	VSS_322	VSS_222	BD116
N188	VSS_323	VSS_223	BD120
N192	VSS_324	VSS_224	BD124
N196	VSS_325	VSS_225	BD128
N200	VSS_326	VSS_226	BD132
N204	VSS_327	VSS_227	BD136
N208	VSS_328	VSS_228	BD140
N212	VSS_329	VSS_229	BD144
N216	VSS_330	VSS_230	BD148
N220	VSS_331	VSS_231	BD152
N224	VSS_332	VSS_232	BD156
N228	VSS_333	VSS_233	BD160
N232	VSS_334	VSS_234	BD164
N236	VSS_335	VSS_235	BD168
N240	VSS_336	VSS_236	BD172
N244	VSS_337	VSS_237	BD176
N248	VSS_338	VSS_238	BD180
N252	VSS_339	VSS_239	BD184
N256	VSS_340	VSS_240	BD188
N260	VSS_341	VSS_241	BD192
N264	VSS_342	VSS_242	BD196
N268	VSS_343	VSS_243	BD200
N272	VSS_344	VSS_244	BD204
N276	VSS_345	VSS_245	BD208
N280	VSS_346	VSS_246	BD212
N284	VSS_347	VSS_247	BD216
N288	VSS_348	VSS_248	BD220
N292	VSS_349	VSS_249	BD224
N296	VSS_350	VSS_250	BD228
N300	VSS_351	VSS_251	BD232
N304	VSS_352	VSS_252	BD236
N308	VSS_353	VSS_253	BD240
N312	VSS_354	VSS_254	BD244
N316	VSS_355	VSS_255	BD248
N320	VSS_356	VSS_256	BD252
N324	VSS_357	VSS_257	BD256
N328	VSS_358	VSS_258	BD260

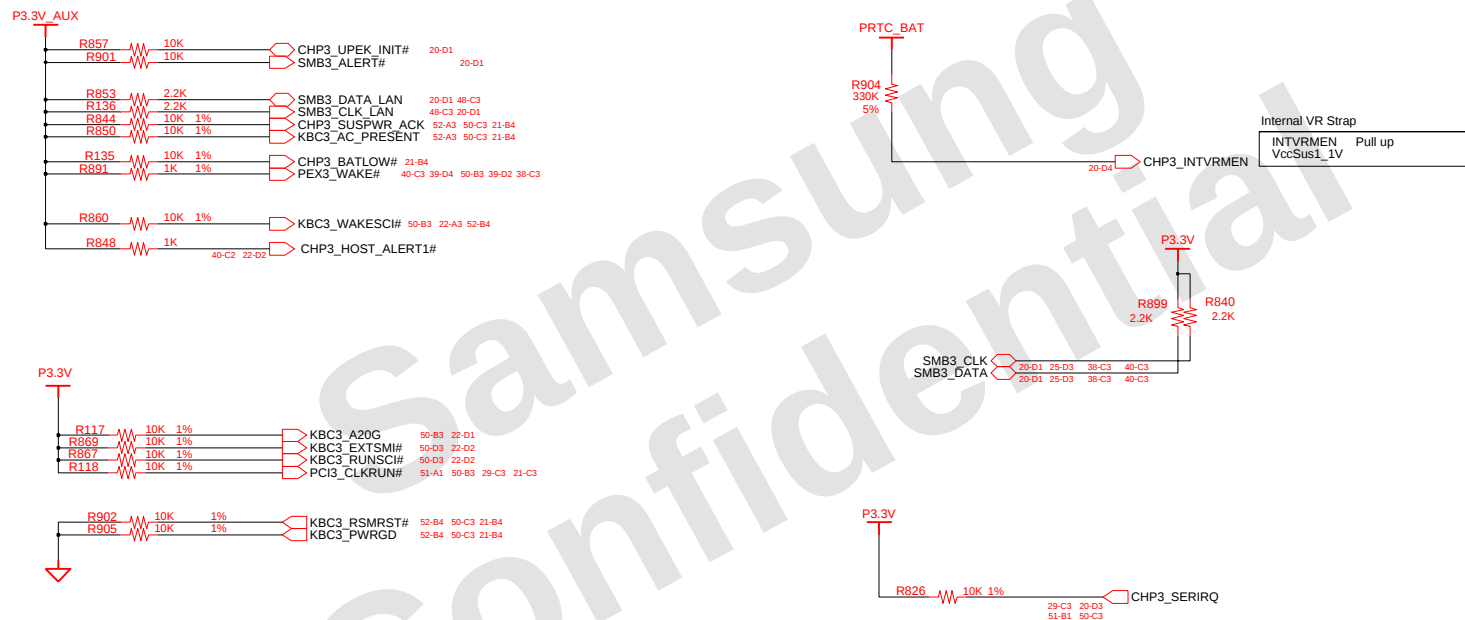
By design guide rev0.8 & Intel Feedback



DESIGN	Xiaohong Zhang	DATE	12/19/2008	TITLE	Suzhou_M	SAMSUNG ELECTRONICS PART NO. BA41-01190/1/2A
CHECK	Rujin Zheng	DEV. STEP	PV		PCH_IBEAX PEAK	
APPROVAL	BC LEE	REV	1.0		PCH_IBEAX PEAK(5/6)	
MODULE CODE		LAST EDIT				
				October 10, 2009 00:22:55 AM	PAGE 20 OF 62	

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For MICOM 80H Debug Port Test

80h_CHP3_SERIRQ_MN

R63 0 Ω noster

P3.3V

J4 HDR-10P-1R-SMD

1 2 3 4 5 6 7 8 9 10 11 12

CHP3_SERIRQ

PLT3_RST#

CLK3_DBG LPC

LPC3_LFRAME#

LPC3_LAD(3)

LPC3_LAD(2)

LPC3_LAD(1)

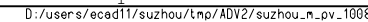
LPC3_LAD(0)

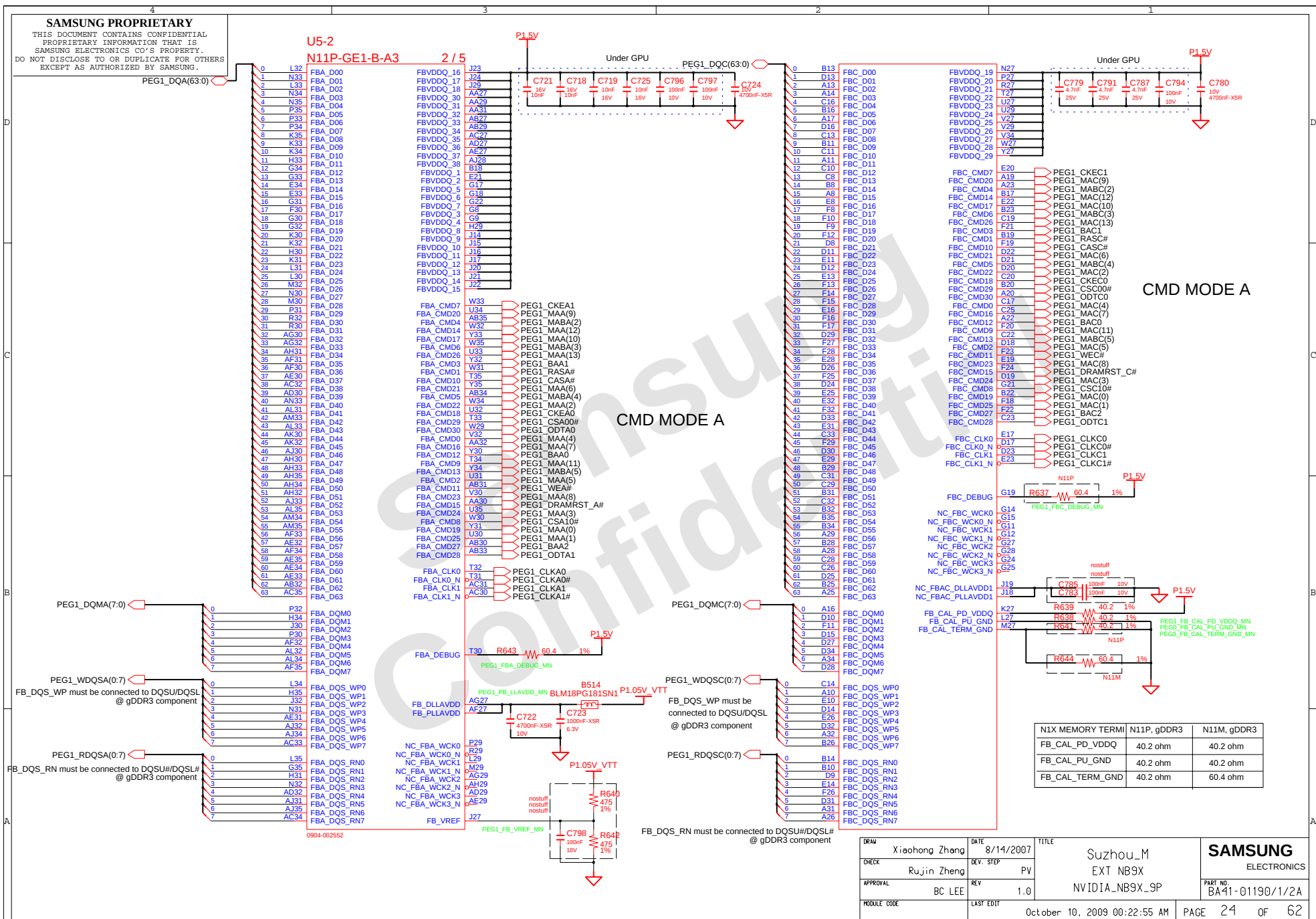
MNT1

MNT2

3711-000386

COM-22C-015(1996.6.5) REV. 3

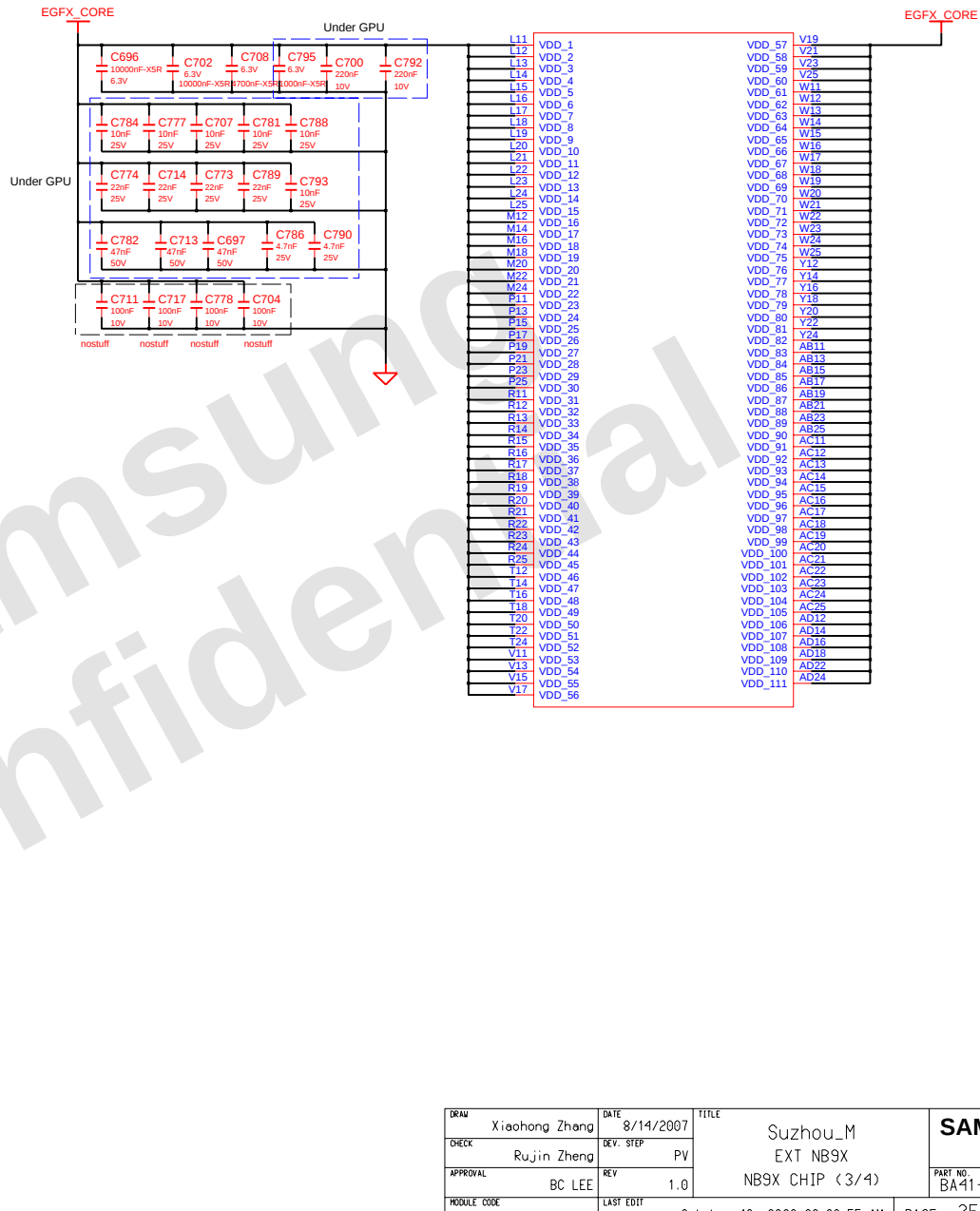




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U5-3
N11P-GE1-B-A3

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Section A: IFPAB Power and Ground

- IFPAB_PLLVDD (A9)
- IFPAB_RSET (A11)
- IFPAB_IOVDD (A9)
- IFPB_IOVDD (A10)

Section B: IFPB Power and Ground

- IFPB_TXD1_N (A9)
- IFPB_TXD1 (A10)
- IFPB_TXD2_N (A10)
- IFPB_TXD2 (A11)
- IFPB_TXD3_N (A11)
- IFPB_TXD3 (A12)
- IFPB_TXC_N (A12)
- IFPB_TXC (A13)
- IFPB_TXD4_N (A13)
- IFPB_TXD4 (A14)
- IFPB_TXD5_N (A14)
- IFPB_TXD5 (A15)
- IFPB_TXD6_N (A15)
- IFPB_TXD6 (A16)
- IFPB_TXD7_N (A16)
- IFPB_TXD7 (A17)
- IFPB_TXC_N (A17)
- IFPB_TXC (A18)

Section C: IFPC Power and Ground

- IFPC_PLLVDD (A7)
- IFPC_RSET (A7)
- IFPC_IOVDD (A8)
- IFPD_PLLVDD (A6)
- IFPD_RSET (A6)
- IFPD_IOVDD (A8)

Section D: IFPD Power and Ground

- IFPD_TXN_HDMI (A4)
- IFPD_TXCP_HDMI (A5)
- IFPD_TXN_HDMI (A6)
- IFPD_TXCP_HDMI (A7)
- IFPD_TXN_HDMI (A8)
- IFPD_TXCP_HDMI (A9)
- IFPD_TXN_HDMI (A10)
- IFPD_TXCP_HDMI (A11)
- IFPD_TXN_HDMI (A12)
- IFPD_TXCP_HDMI (A13)
- IFPD_TXN_HDMI (A14)
- IFPD_TXCP_HDMI (A15)
- IFPD_TXN_HDMI (A16)
- IFPD_TXCP_HDMI (A17)
- IFPD_TXN_HDMI (A18)
- IFPD_TXCP_HDMI (A19)

Section E: IFPEF Power and Ground

- IFPEF_PLLVDD (A1)
- IFPEF_RSET (A1)
- IFPEF_IOVDD (A7)
- IFPF_IOVDD (A7)

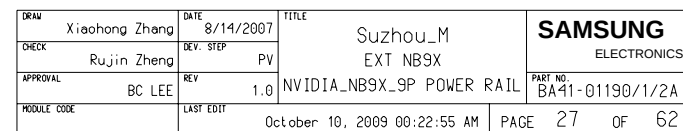
Section F: IFPF Power and Ground

- IFPF_TXN_HDMI (A1)
- IFPF_TXCP_HDMI (A2)
- IFPF_TXN_HDMI (A3)
- IFPF_TXCP_HDMI (A4)
- IFPF_TXN_HDMI (A5)
- IFPF_TXCP_HDMI (A6)
- IFPF_TXN_HDMI (A7)
- IFPF_TXCP_HDMI (A8)
- IFPF_TXN_HDMI (A9)
- IFPF_TXCP_HDMI (A10)
- IFPF_TXN_HDMI (A11)
- IFPF_TXCP_HDMI (A12)
- IFPF_TXN_HDMI (A13)
- IFPF_TXCP_HDMI (A14)
- IFPF_TXN_HDMI (A15)
- IFPF_TXCP_HDMI (A16)
- IFPF_TXN_HDMI (A17)
- IFPF_TXCP_HDMI (A18)
- IFPF_TXN_HDMI (A19)
- IFPF_TXCP_HDMI (A20)

Module Connector Pinout

- IFPAB_TXD1_N (A9)
- IFPAB_TXD1 (A10)
- IFPAB_TXD2_N (A10)
- IFPAB_TXD2 (A11)
- IFPAB_TXD3_N (A11)
- IFPAB_TXD3 (A12)
- IFPAB_TXC_N (A12)
- IFPAB_TXC (A13)
- IFPAB_TXD4_N (A13)
- IFPAB_TXD4 (A14)
- IFPAB_TXD5_N (A14)
- IFPAB_TXD5 (A15)
- IFPAB_TXD6_N (A15)
- IFPAB_TXD6 (A16)
- IFPAB_TXD7_N (A16)
- IFPAB_TXD7 (A17)
- IFPAB_TXC_N (A17)
- IFPAB_TXC (A18)
- IFPC_PLLVDD (A7)
- IFPC_RSET (A7)
- IFPC_IOVDD (A8)
- IFPD_PLLVDD (A6)
- IFPD_RSET (A6)
- IFPD_IOVDD (A8)
- IFPD_TXN_HDMI (A4)
- IFPD_TXCP_HDMI (A5)
- IFPD_TXN_HDMI (A6)
- IFPD_TXCP_HDMI (A7)
- IFPD_TXN_HDMI (A8)
- IFPD_TXCP_HDMI (A9)
- IFPD_TXN_HDMI (A10)
- IFPD_TXCP_HDMI (A11)
- IFPD_TXN_HDMI (A12)
- IFPD_TXCP_HDMI (A13)
- IFPD_TXN_HDMI (A14)
- IFPD_TXCP_HDMI (A15)
- IFPD_TXN_HDMI (A16)
- IFPD_TXCP_HDMI (A17)
- IFPD_TXN_HDMI (A18)
- IFPD_TXCP_HDMI (A19)
- IFPEF_PLLVDD (A1)
- IFPEF_RSET (A1)
- IFPEF_IOVDD (A7)
- IFPF_IOVDD (A7)
- IFPF_TXN_HDMI (A1)
- IFPF_TXCP_HDMI (A2)
- IFPF_TXN_HDMI (A3)
- IFPF_TXCP_HDMI (A4)
- IFPF_TXN_HDMI (A5)
- IFPF_TXCP_HDMI (A6)
- IFPF_TXN_HDMI (A7)
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- IFPF_TXCP_HDMI (A10)
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- IFPF_TXCP_HDMI (A16)
- IFPF_TXN_HDMI (A17)
- IFPF_TXCP_HDMI (A18)
- IFPF_TXN_HDMI (A19)
- IFPF_TXCP_HDMI (A20)

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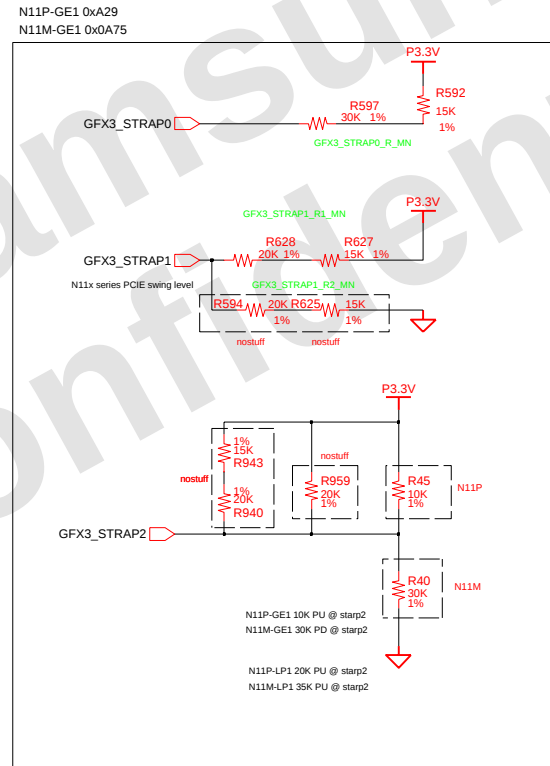
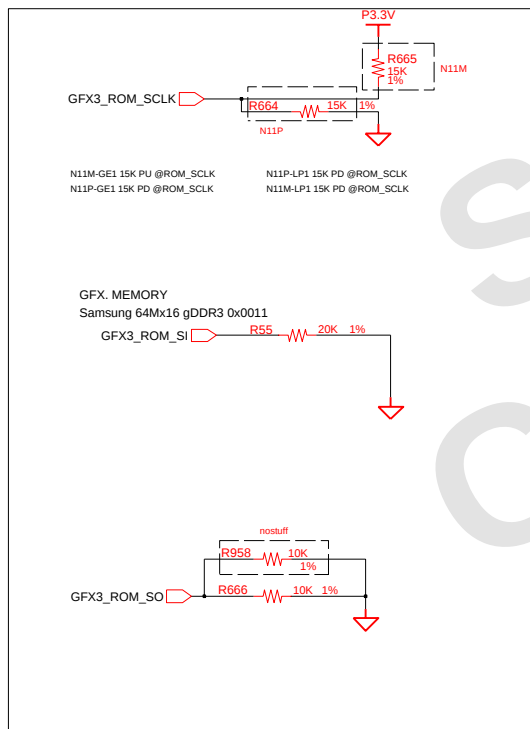


N11x_40nm STRAP

Pin	Description	Activate	Pin	Description	Activate
GPIO(0)	General Purpose	NC	GPIO(12)	PWR_LEVEL	NC
GPIO(1)	HPD-C	NC	GPIO(13)	MEM_VID	NC
GPIO(2)	LCD0_BL_PWM	High	GPIO(14)	PWR_CTRL1	NC
GPIO(3)	LCD0_VDD	High	GPIO(15)	HPD-E	High
GPIO(4)	LCD0_BL_EN	High	GPIO(16)	FAN_PWM	NC
GPIO(5)	GPU_VID0	00 0.8v 10 0.95v	GPIO(17)	Reserved	NC
GPIO(6)	GPU_VID1	01 0.85v 11 1.03v	GPIO(18)	Reserved	NC
GPIO(7)	GPU_VID2	NC	GPIO(19)	HPD-D	NC
GPIO(8)	OVERT	LOW			
GPIO(9)	ALERT	NC			
GPIO(10)	MEM_VREF	NC			
GPIO(11)	SLI_SYNC	NC			

STRAP PIN	BIT 3	BIT 2	BIT 1	BIT0
ROM_SO	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]

RESISTOR	PULL UP	PULL DOWN
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111



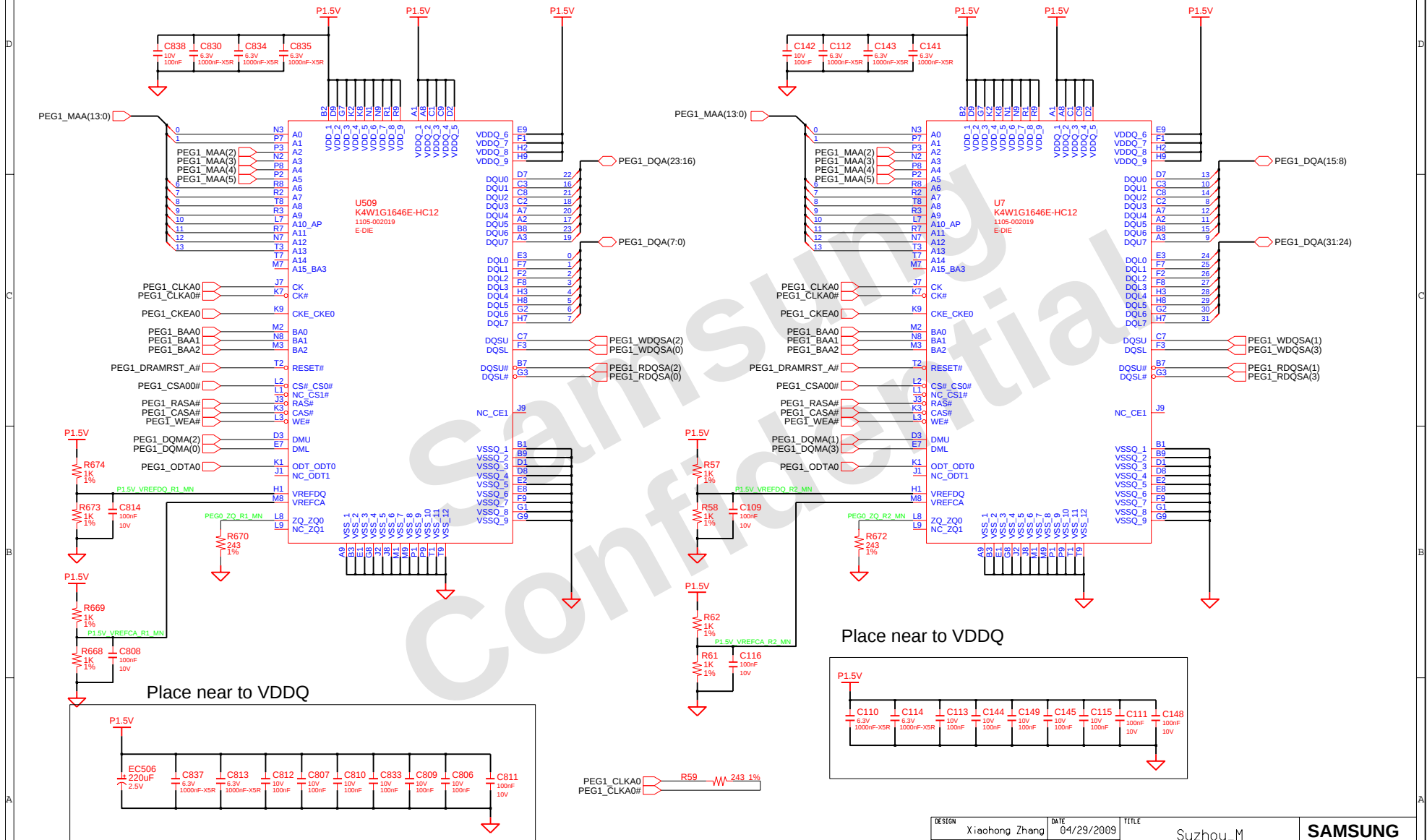
	Bit3	Bit2	Bit1	Bit0	
ROMSO	0	0	0	1	27M
SCLK	0	0	1	0	DEVICE ID GFX TPYE
SI	0	0	1	1	gDDR3 1Gb
Strap2	1	0	0	1	N11P-GE1 DEVICE ID
Strap1	1	1	1	0	PEG PCIE swing level
Strap0	1	1	1	1	EDID_EN

N11P-GE1 0x0A29

	Bit3	Bit2	Bit1	Bit0	
ROMSO	0	0	0	1	27M
SCLK	0	0	1	0	DEVICE ID GFX TPYE
SI	0	0	1	1	gDDR3 1Gb
Strap2	0	1	0	1	N11P-GE1 DEVICE ID
Strap1	1	1	1	0	PEG PCIE swing level
Strap0	1	1	1	1	EDID_EN

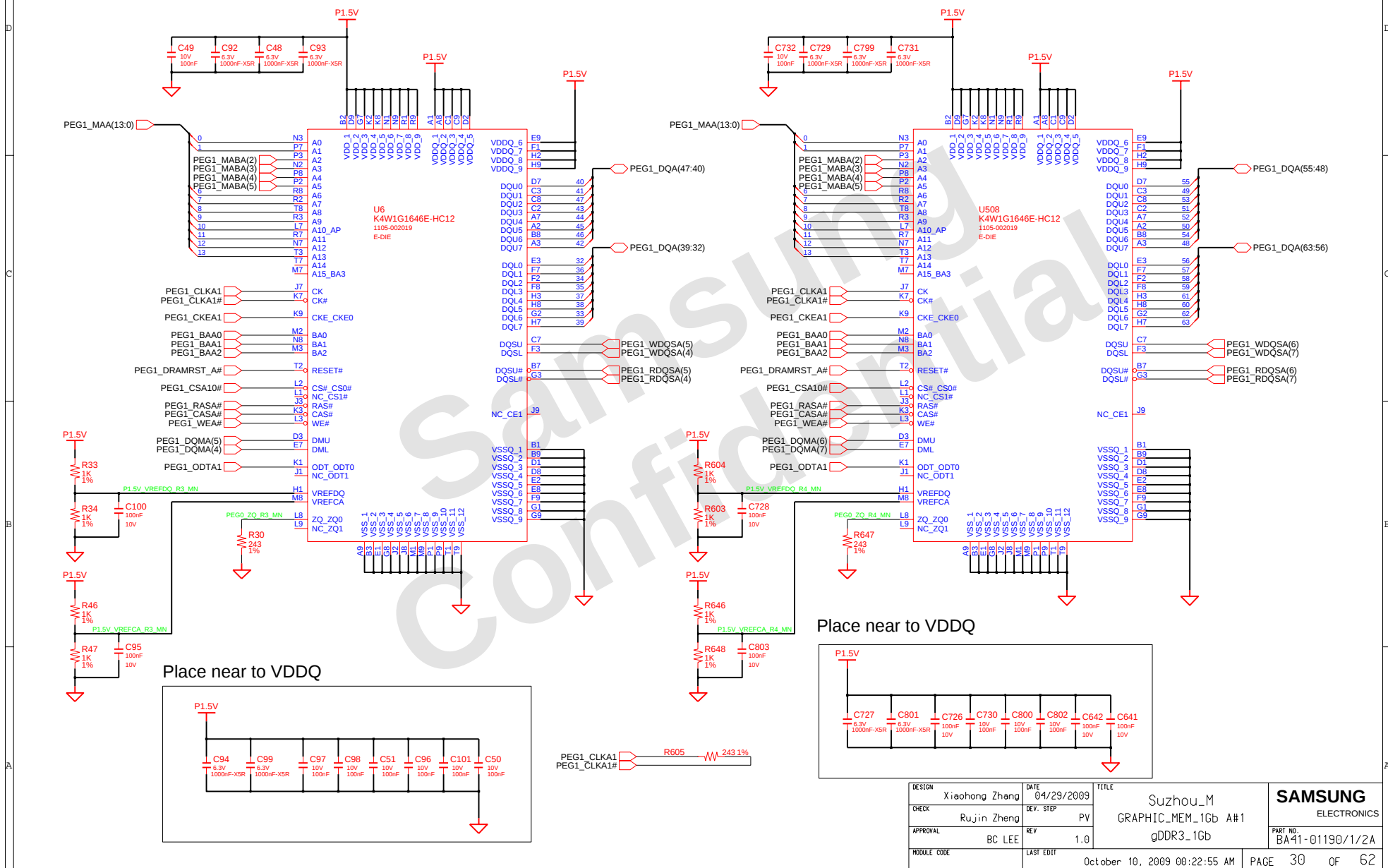
N11M-GE1 0x0A75

A-Channel #0



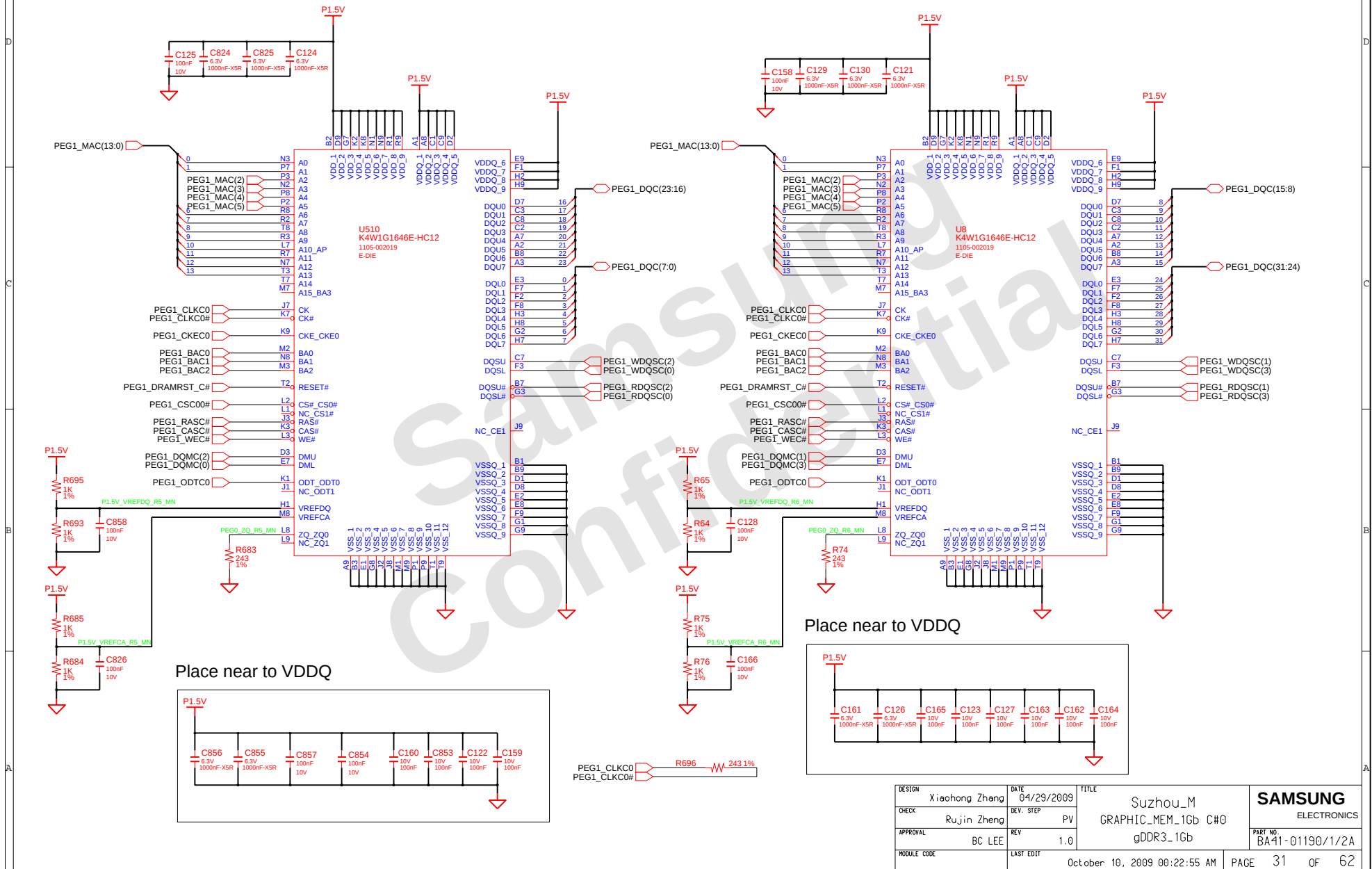
DESIGN	Xiaohong Zhang	DATE	04/29/2009	TITLE	Suzhou_M	SAMSUNG ELECTRONICS PART NO. BA41-01190/1/2A
CHECK	Rujin Zheng	DEV. STEP	PV		GRAPHIC_MEM_1Gb A#0	
APPROVAL	BC LEE	REV	1.0		gDDR3_1Gb	
MODULE CODE		LAST EDIT				
				October 10, 2009 00:22:55 AM	PAGE	29 OF 62

A-Channel #1



C-Channel #0

N11P

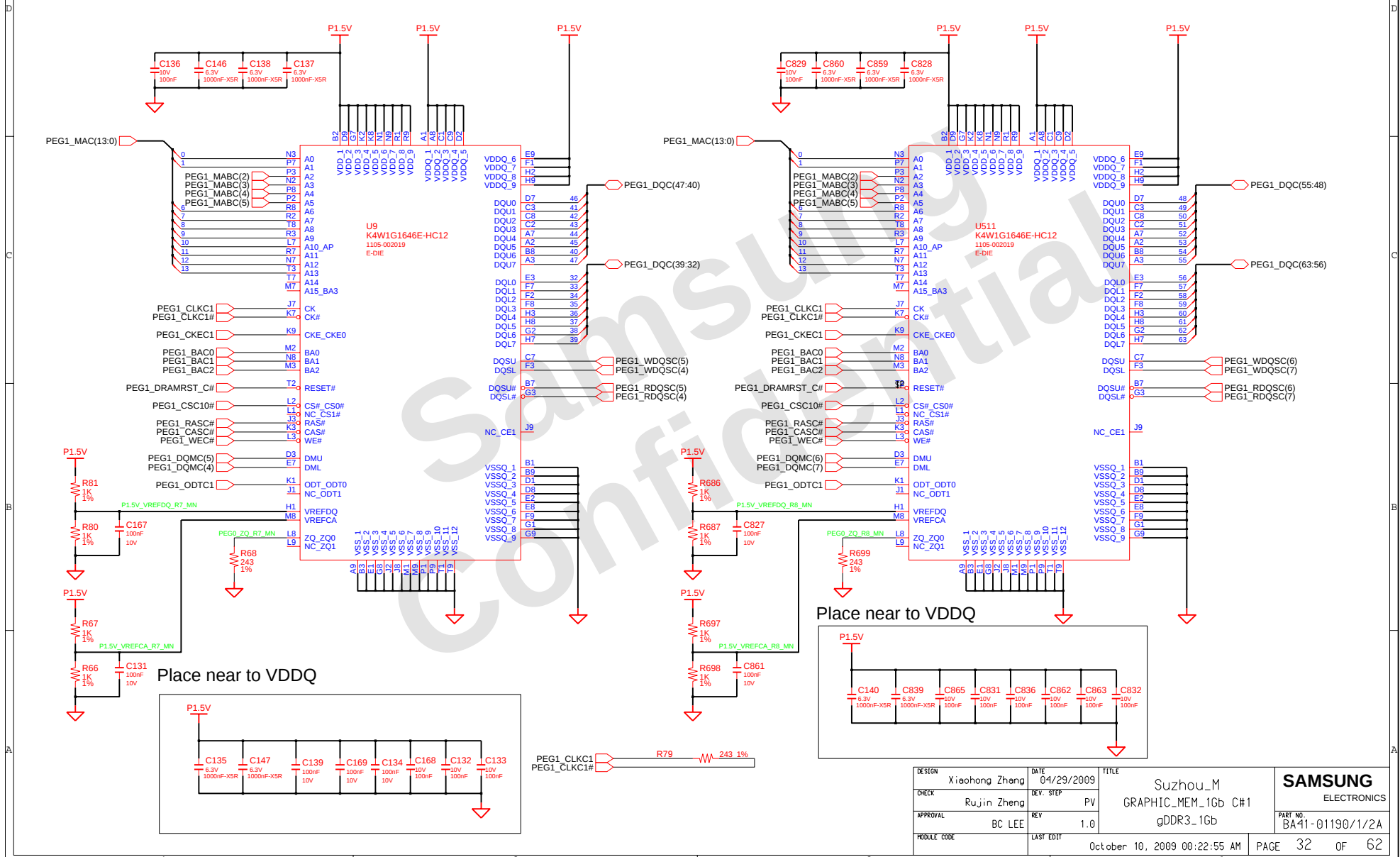


DESIGN	Xiaohong Zhang	DATE	04/29/2009	TITLE	Suzhou_M
CHECK	Rujin Zheng	DEV. STEP	PV		GRAPHIC_MEM_1Gb C#0
APPROVAL	BC LEE	REV	1.0		gDDR3_1Gb
MODULE CODE		LAST EDIT	October 10, 2009 00:22:55 AM	PAGE	31 OF 62

SAMSUNG
ELECTRONICS
PART NO.
BA41-01190/1/2A

C-Channel #1

N11P



DESIGN	Xiaohong Zhang	DATE	04/29/2009	TITLE	Suzhou_M	SAMSUNG ELECTRONICS PART NO. BA41-01190/1/2A
CHECK	Rujin Zheng	DEV. STEP	PV		GRAPHIC_MEM_1Gb C#1	
APPROVAL	BC LEE	REV	1.0		gDDR3-1Gb	
MODULE CODE		LAST EDIT	October 10, 2009 00:22:55 AM	PAGE	32 OF 62	

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gDDR3 Memory PULL UP & PULL DOWN

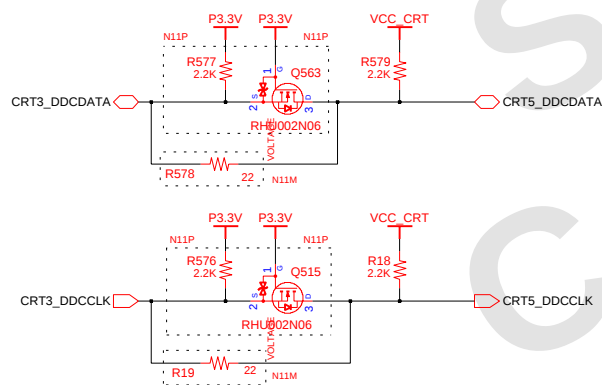
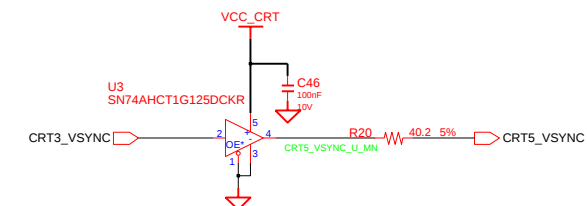
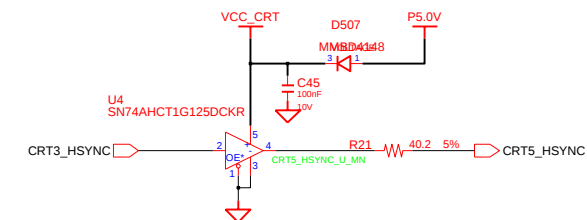


DESIGN	Xiaohong Zhang	DATE	03/14/2009	TITLE	Suzhou_M PULL-UP&PULL-DOWN gDDR3_1Gb	SAMSUNG ELECTRONICS PART NO. BA41-01190/1/2A
CHECK	Rujin Zheng	DEV. STEP	PV			
APPROVAL	BC LEE	REV	1.0			
MODULE CODE	LAST EDIT		October 10, 2009 00:22:55 AM	PAGE 33	OF 62	

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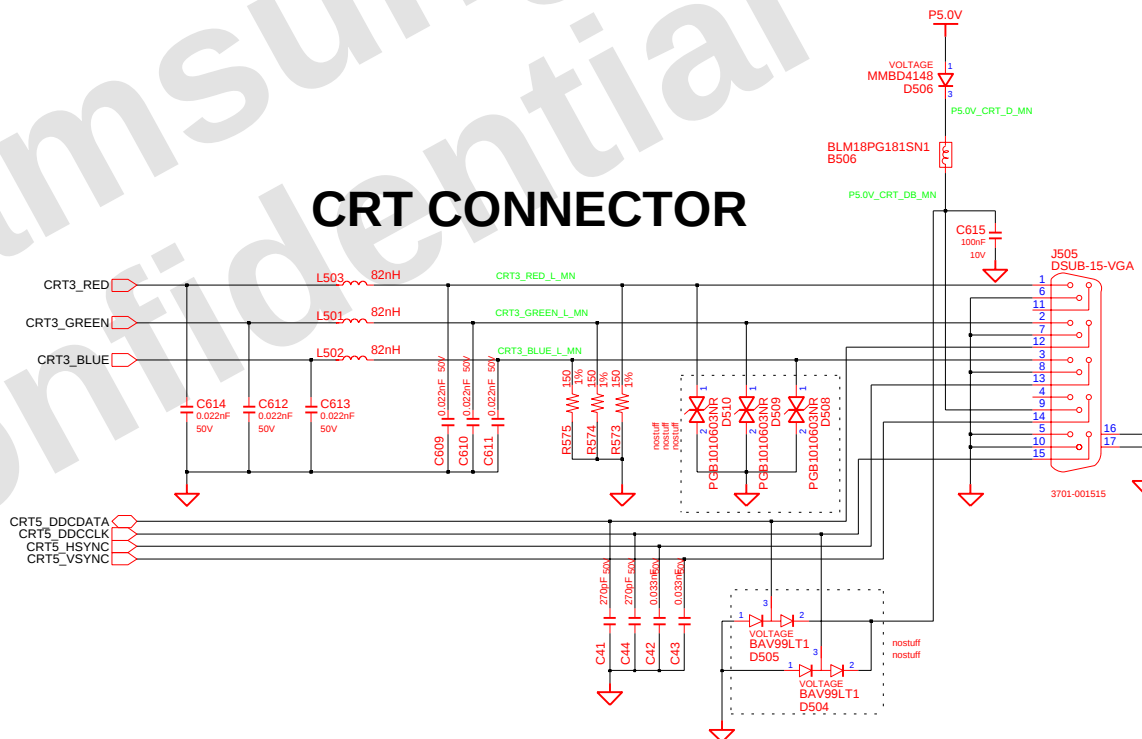
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CRT



Check "CRT3_DDCCLK/DATA" Voltage Level
2N06 Can be replaced with SM6K2

CRT CONNECTOR



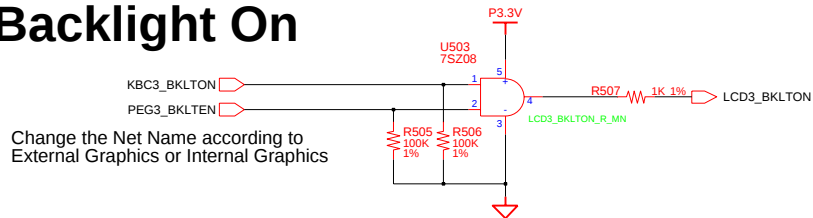
DESIGN	Xiaohong Zhang	DATE	01/08/2009	TITLE	Suzhou_M GRAPHICS_IF CRT	SAMSUNG ELECTRONICS PART NO. BA41-01190/1/2A
CHECK	Rujin Zheng	DEV. STEP	PV			
APPROVAL	BC LEE	REV	1.0			
MODULE CODE		LAST EDIT	October 10, 2009 00:22:55 AM	PAGE	34 OF 62	

LVDS

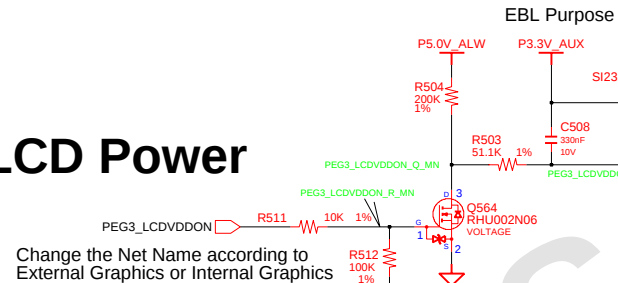
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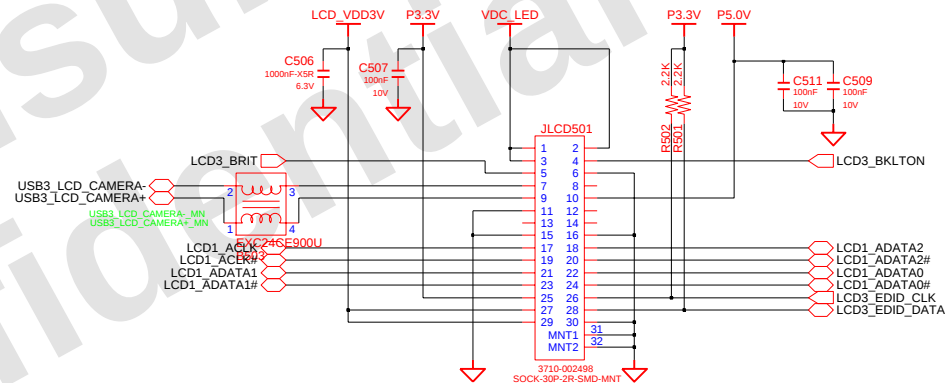
Backlight On



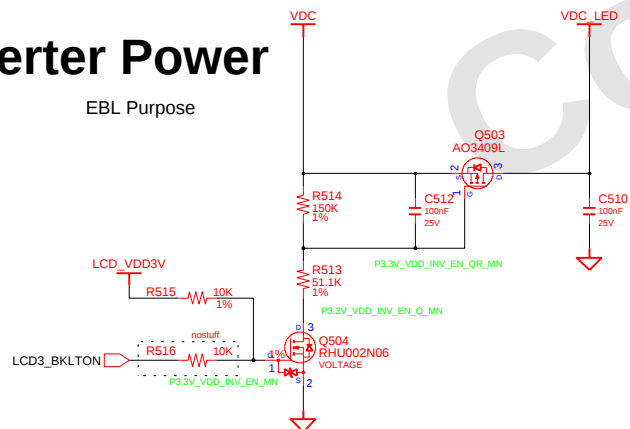
LCD Power



1Ch. LCD Connector



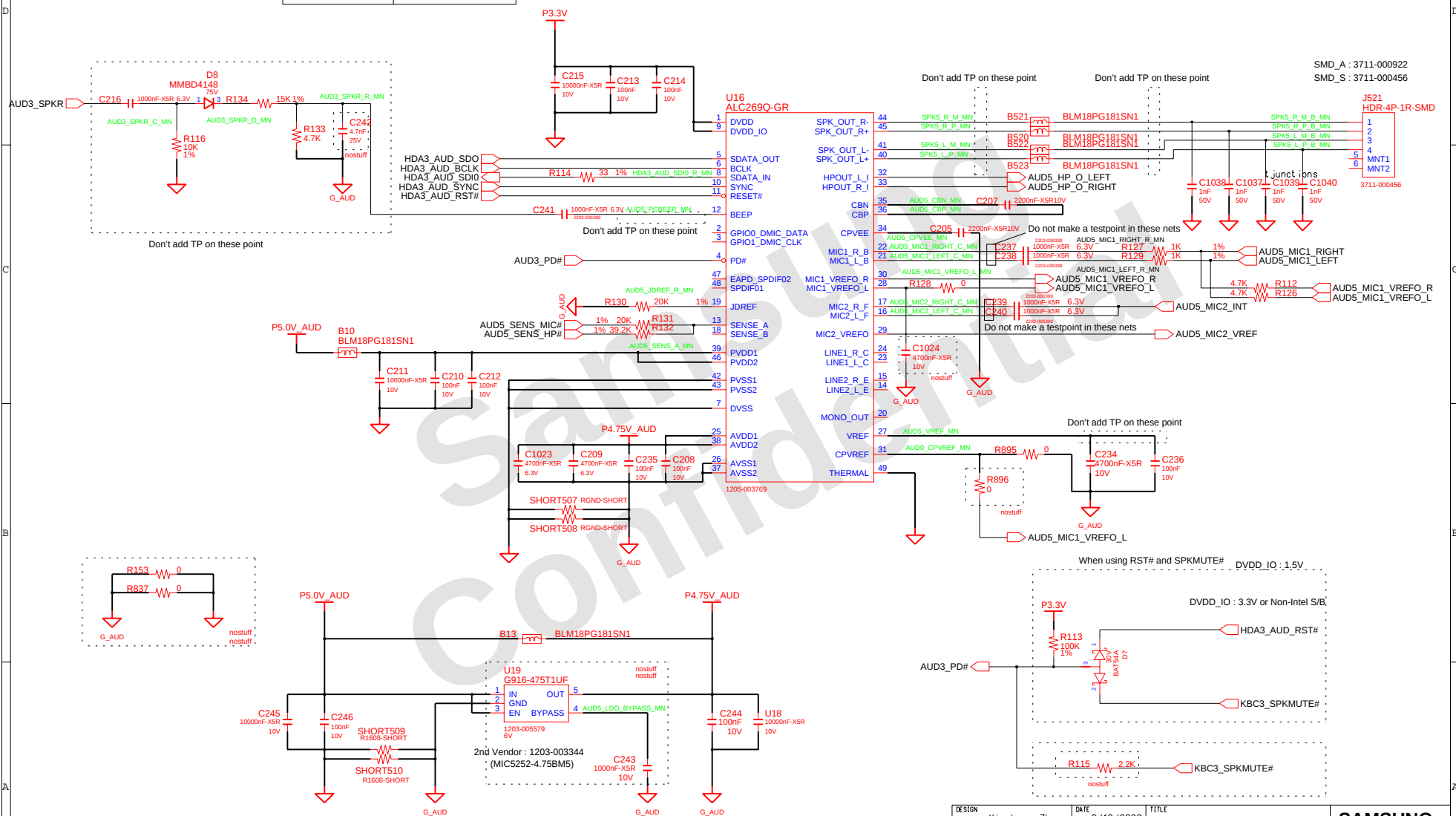
Inverter Power



DESIGN	Xiaohong Zhang	DATE	01/08/2009	TITLE	Suzhou_M GRAPHICS_IF LVDS	SAMSUNG ELECTRONICS
CHECK	Rujin Zheng	DEV. STEP	PV			PART NO. BA41-01190/1/2A
APPROVAL	BC LEE	REV	1.0			
MODULE CODE		LAST EDIT	October 10, 2009 00:22:55 AM	PAGE	35	OF 62

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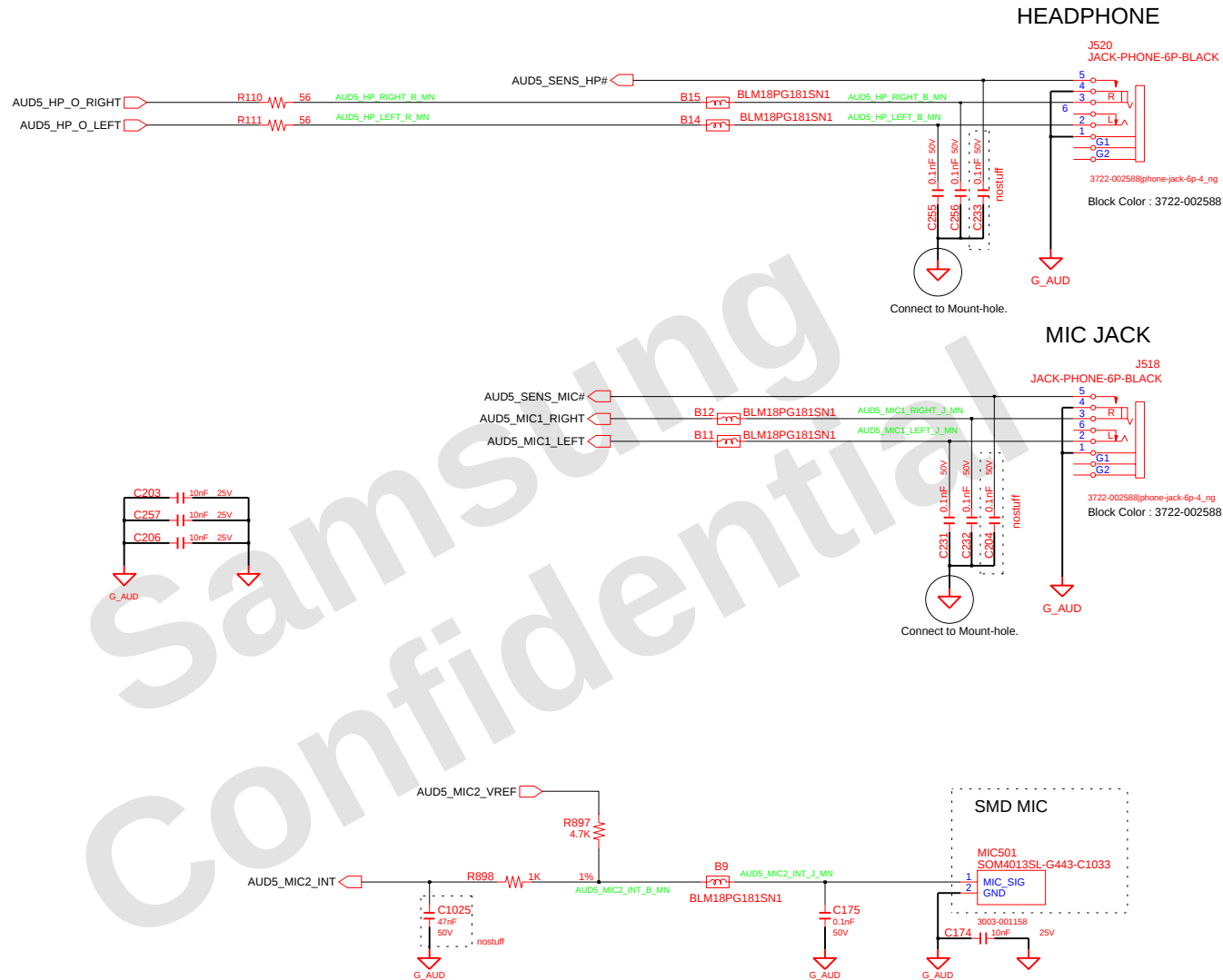
Codec Pin9 Setting	
S/B with Low Voltage IO	S/B without Low Voltage IO
Pin9 : 1.5V	Pin9 : 3.3V



DESIGN	Xiaohong Zhang	DATE	3/13/2009	TITLE	Suzhou_M HDA_ALC269_GR AUDIO CODEC	SAMSUNG ELECTRONICS
CHECK	Rujin Zheng	DEV. STEP	PV			
APPROVAL	BC LEE	REV	1.0			
MODULE CODE	LAST EDIT		October 10, 2009 00:22:55 AM			
				PART NO.	BA41-01190/1/2A	

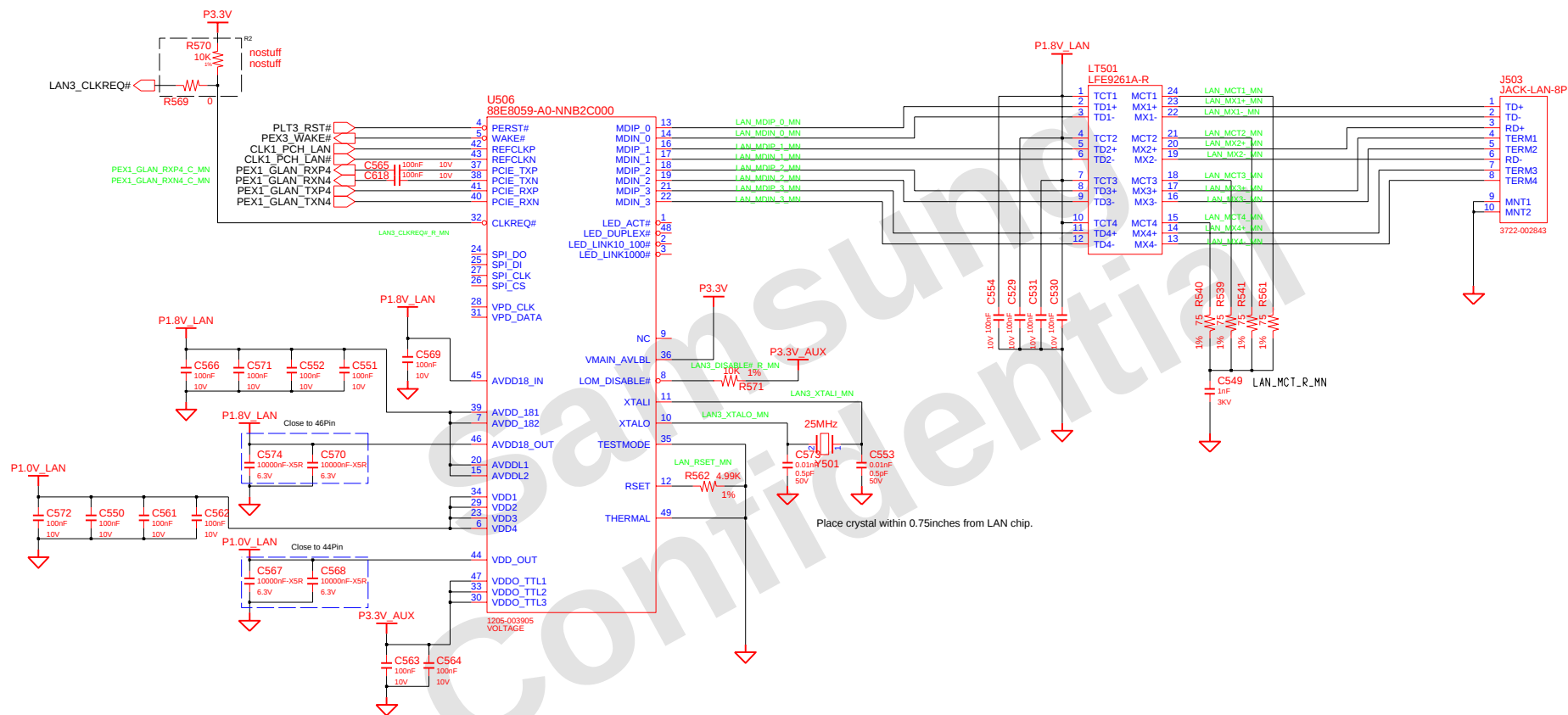
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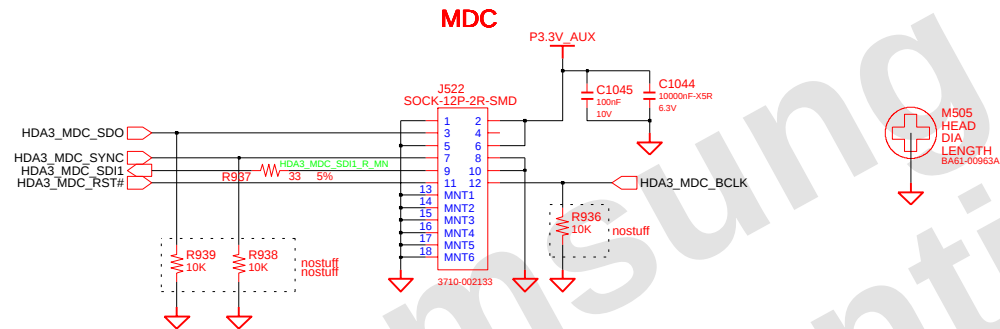
DESIGN	Xiaohong Zhang	DATE	3/13/2009	TITLE	Suzhou_M	SAMSUNG ELECTRONICS PART NO. BA41-01190/1/2A
CHECK	Rujin Zheng	DEV. STEP	PV		HDA_ALC269_GR	
APPROVAL	BC LEE	REV	1.0		AUDIO INPUT/OUTPUT	
MODULE CODE		LAST EDIT	October 10, 2009 00:22:55 AM	PAGE	38 OF 62	

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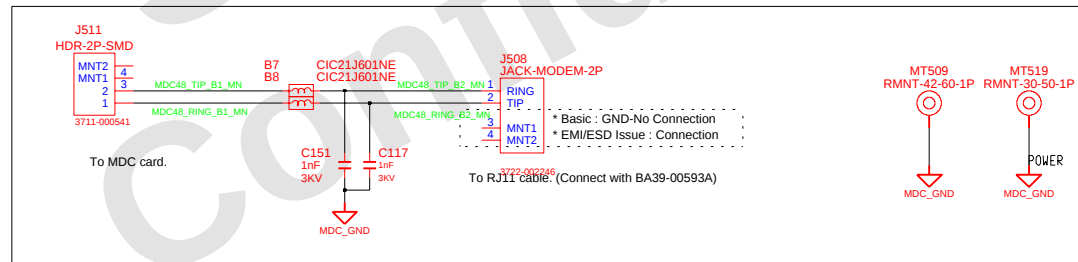


DESIGN	Xiaohong Zhang	DATE	10/6/2008	TITLE	Suzhou_M	SAMSUNG ELECTRONICS	
CHECK	Rujin Zheng	DEV. STEP	PV				
APPROVAL	BC LEE	REV	1.0				
MODULE CODE	LAST EDIT		October 10, 2009 00:22:55 AM				PAGE
				PART NO.		BA41-01190/1/2A	

MDC Connector



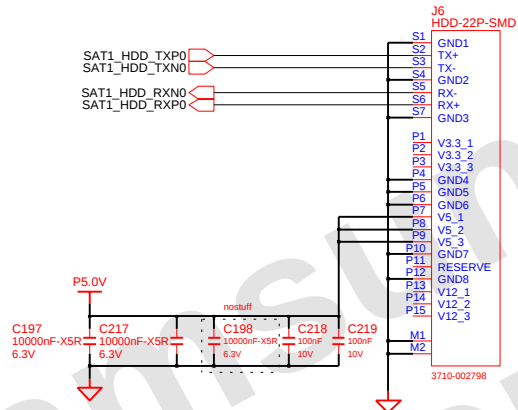
MDC SUB



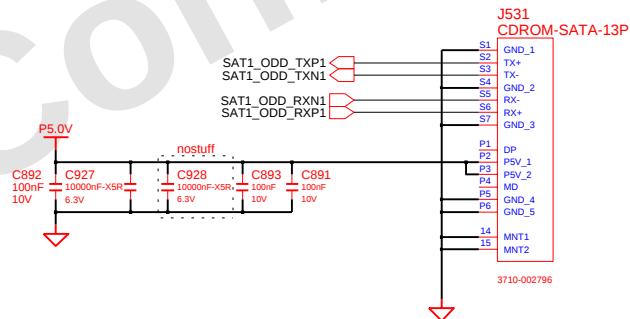
DESIGN	Xiaohong Zhang	DATE	8/20/2009	TITLE	Suzhou_M	SAMSUNG ELECTRONICS
CHECK	Rujin Zheng	DEV. STEP	PV		UNDEFINED	
APPROVAL	BC LEE	REV	1.0		UNDEFINED	
MODULE CODE		LAST EDIT	October 10, 2009 00:22:55 AM	PAGE	40	OF 62

SATA I/F CONN

SATA HDD CONN

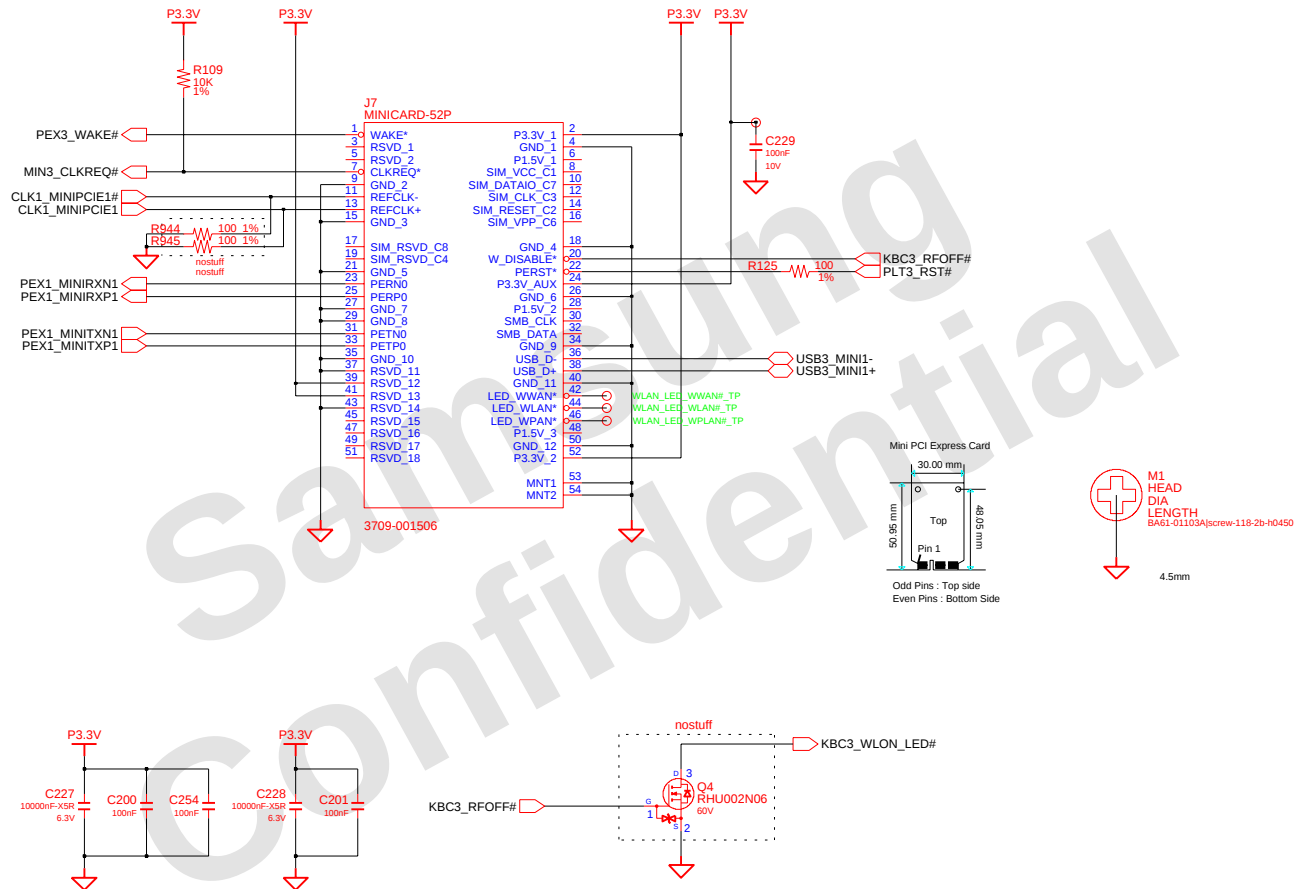


SATA ODD CONN



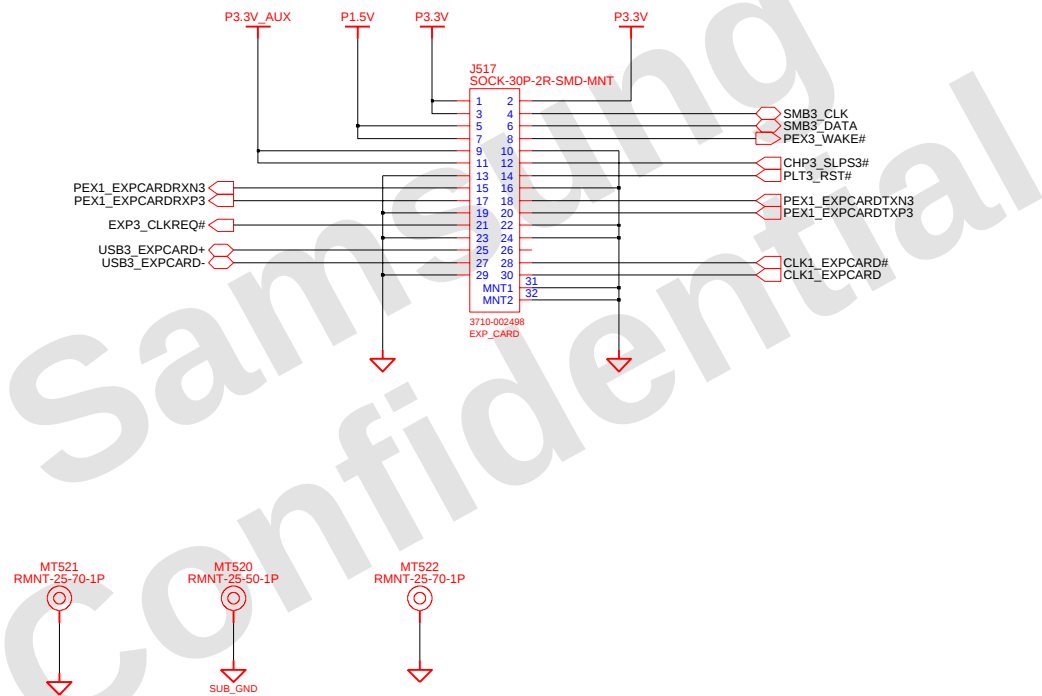
DESIGN	Xiaohong Zhang	DATE	6/6/2008	TITLE	Suzhou_M SATA_DEVICES	SAMSUNG ELECTRONICS PART NO. BA41-01190/1/2A
CHECK	Rujin Zheng	DEV. STEP	PV			
APPROVAL	BC LEE	REV	1.0			
MODULE CODE		LAST EDIT	October 10, 2009 00:22:55 AM	PAGE	41 OF 62	

WLAN, 7mm



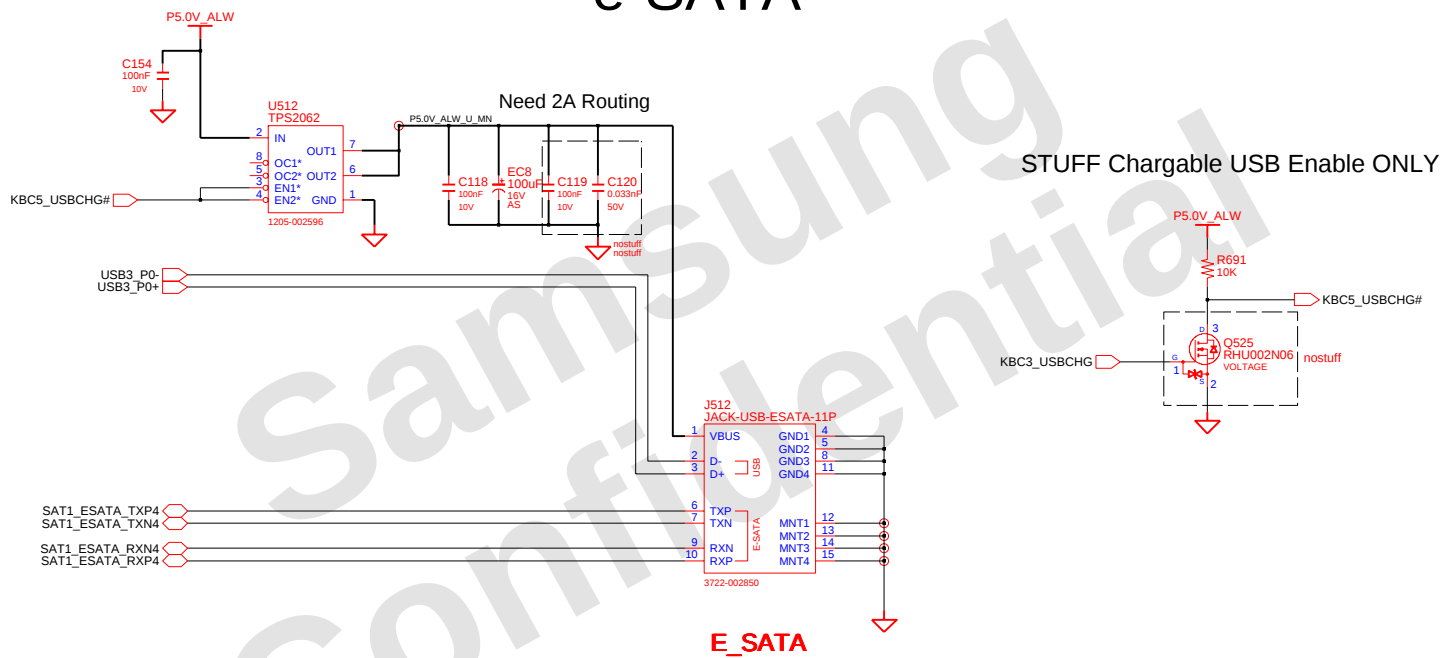
DESIGN	Xiaohong Zhang	DATE	6/6/2008	TITLE	Suzhou_M MINI_PCIE_CONN	SAMSUNG ELECTRONICS PART NO. BA41-01190/1/2A
CHECK	Rujin Zheng	DEV. STEP	PV			
APPROVAL	BC LEE	REV	1.0			
MODULE CODE		LAST EDIT	October 10, 2009 00:22:55 AM	PAGE	42 OF 62	

Express Card



DESIGN	Xiaohong Zhang	DATE	7/7/2008	TITLE	Suzhou_M EXPRESS CARD	SAMSUNG ELECTRONICS PART NO. BA41-01190/1/2A
CHECK	Rujin Zheng	DEV. STEP	PV			
APPROVAL	BC LEE	REV	1.0			
MODULE CODE		LAST EDIT	October 10, 2009 00:22:55 AM	PAGE	43 OF 62	

e-SATA

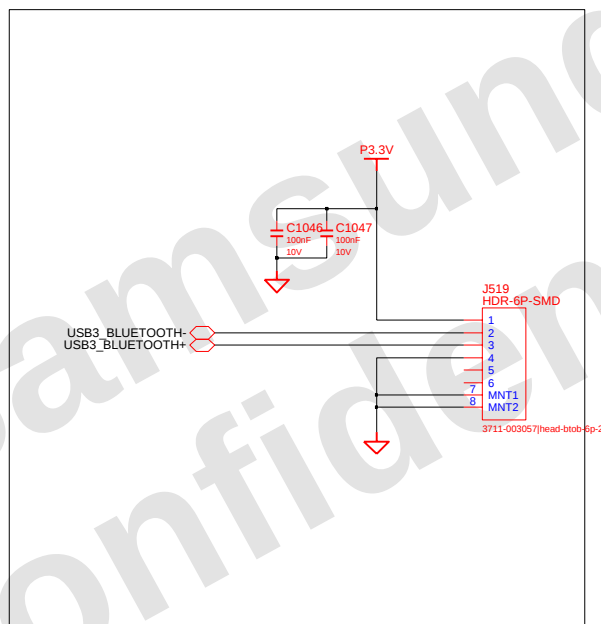


DRAW	Xiaohong Zhang	DATE	11/8/2006	TITLE	Suzhou_M MINI CARD SILOH & EBON	SAMSUNG ELECTRONICS
CHECK	Rujin Zheng	DEV. STEP	PV			
APPROVAL	BC LEE	REV	1.0			
MODULE CODE		LAST EDIT		October 10, 2009 00:22:55 AM	PAGE	44 OF 62

USB I/F Devices

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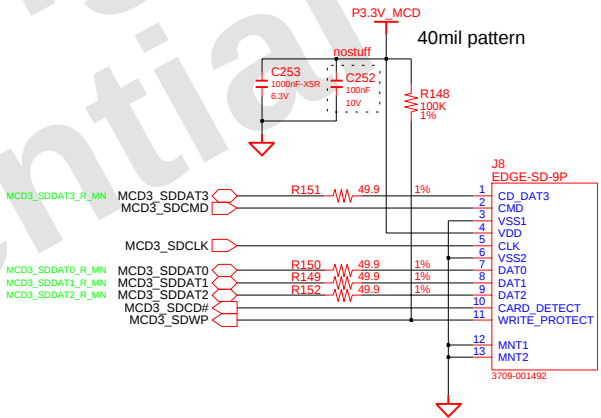
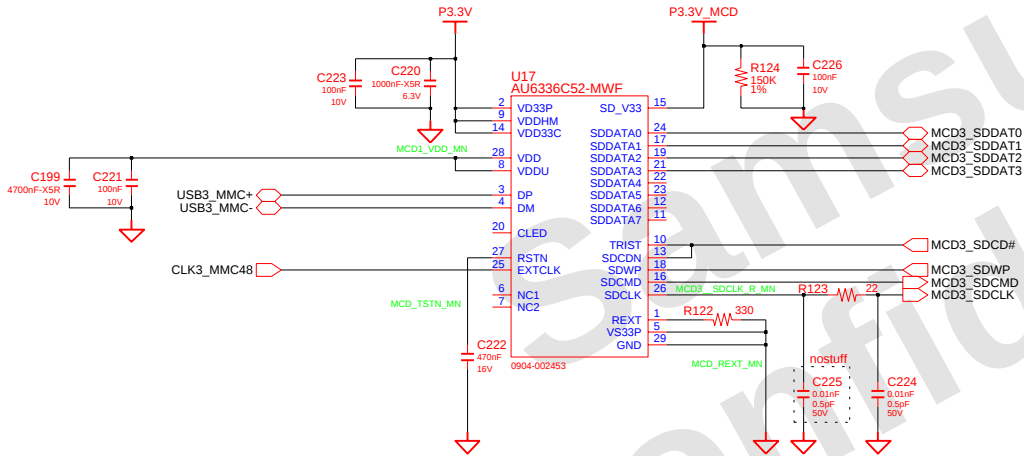
Bluetooth Interface



DESIGN	Xiaohong Zhang	DATE	6/6/2008	TITLE Suzhou_M USB_DEVICES	SAMSUNG ELECTRONICS
CHECK	Rujin Zheng	DEV. STEP	PV		
APPROVAL	BC LEE	REV	1.0		
MODULE CODE	LAST EDIT		October 10, 2009 00:22:55 AM		
				PART NO.	BA41-01190/1/2A

3 IN 1

P3.3V_MCD distance between R5U880 and socket should be less than 2 inches

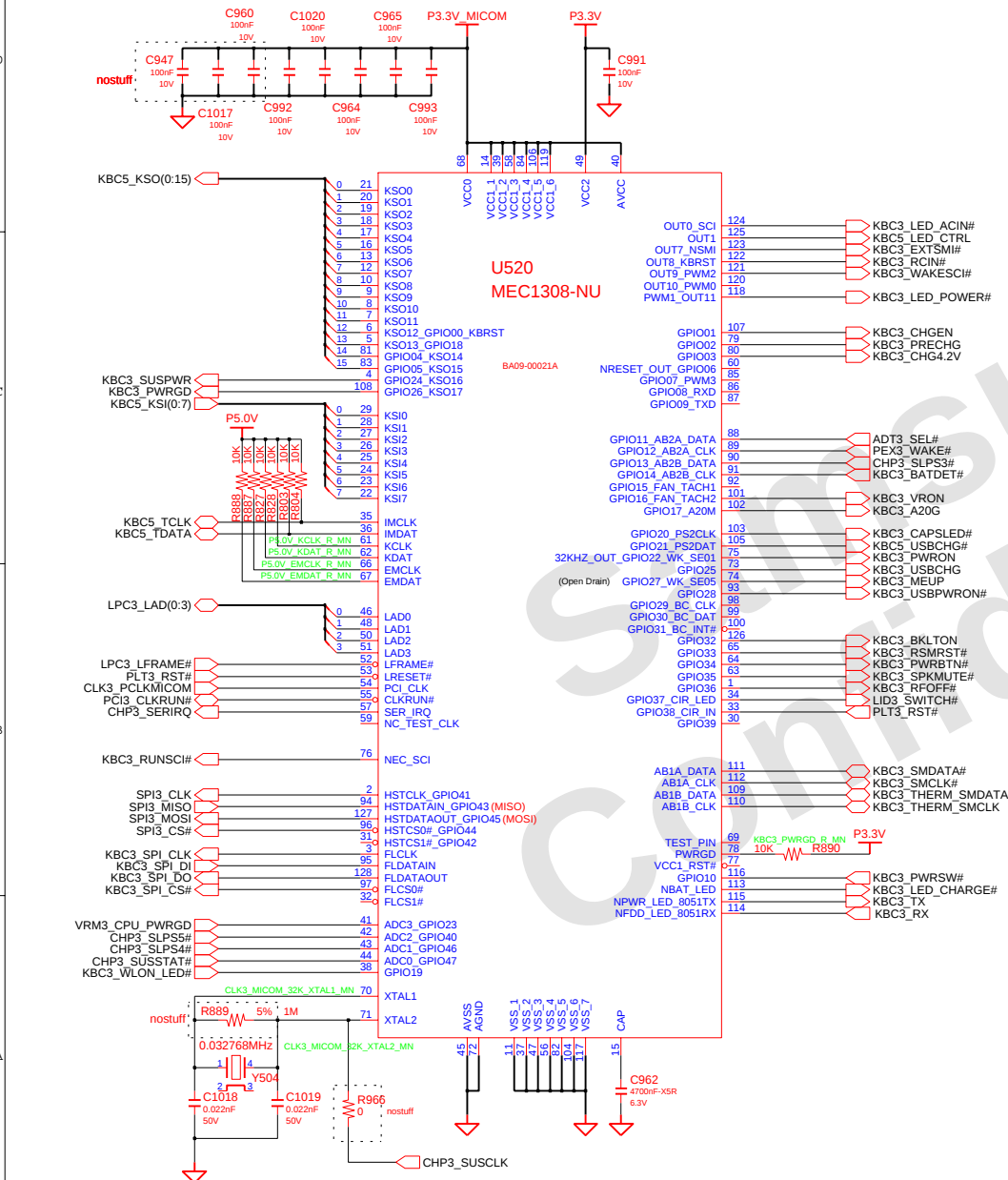


40 mil trace for medica card socket ground

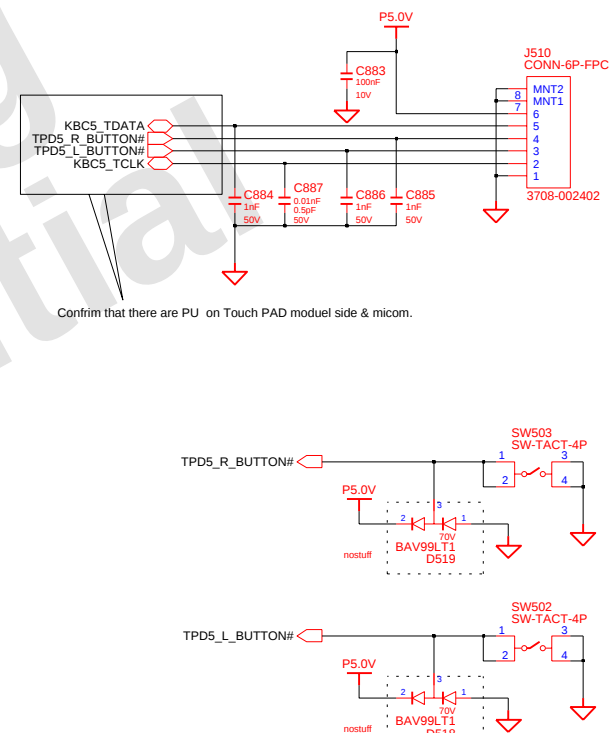
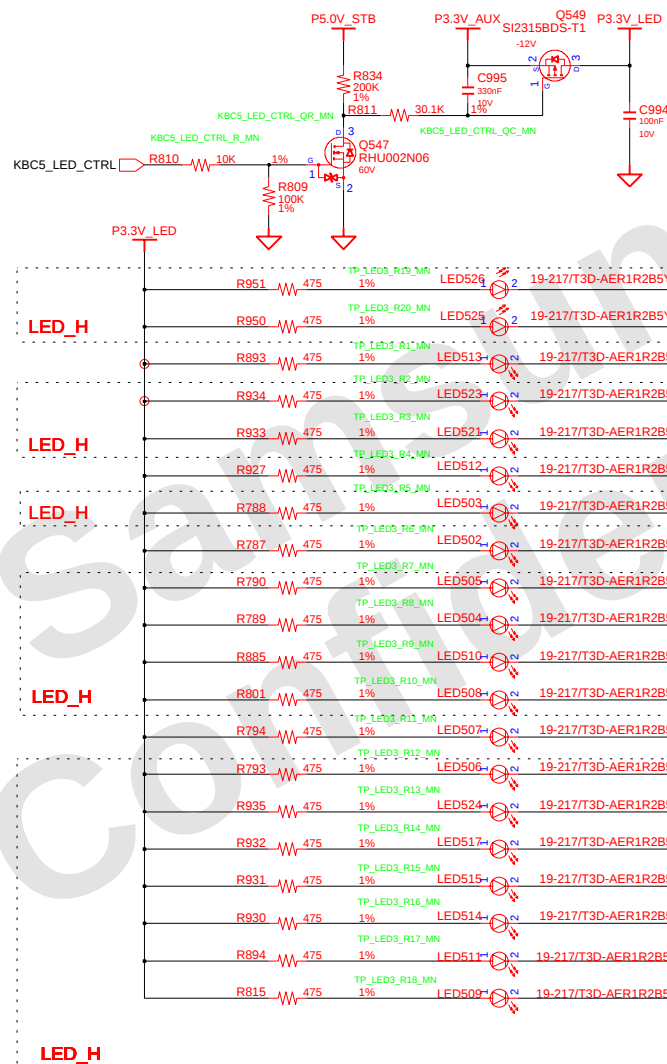
MSEL5	SD Write Protec Selection
Connected to VCC	High Enable
Connected to GND	Low Enable
MSEL7	PLL BASE CLOCK SELECTION
Connected to VCC	12MHz
Connected to GND	48MHz

DESIGN	Xiaohong Zhang	DATE	10/15/2008	TITLE	Suzhou_M	SAMSUNG ELECTRONICS PART NO. BA41-01190/1/2A
CHECK	Rujin Zheng	DEV. STEP	PV		MMC	
APPROVAL	BC LEE	REV	1.0		AU6336	
MODULE CODE		LAST EDIT	October 10, 2009 00:22:55 AM	PAGE	46 OF 62	

MAIN BOARD (MICOM)



TOUCHPAD



COM-22C-015(1996.6.5) REV. 3

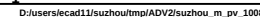
LED SWITCH LOGIC

Function Key LEDS



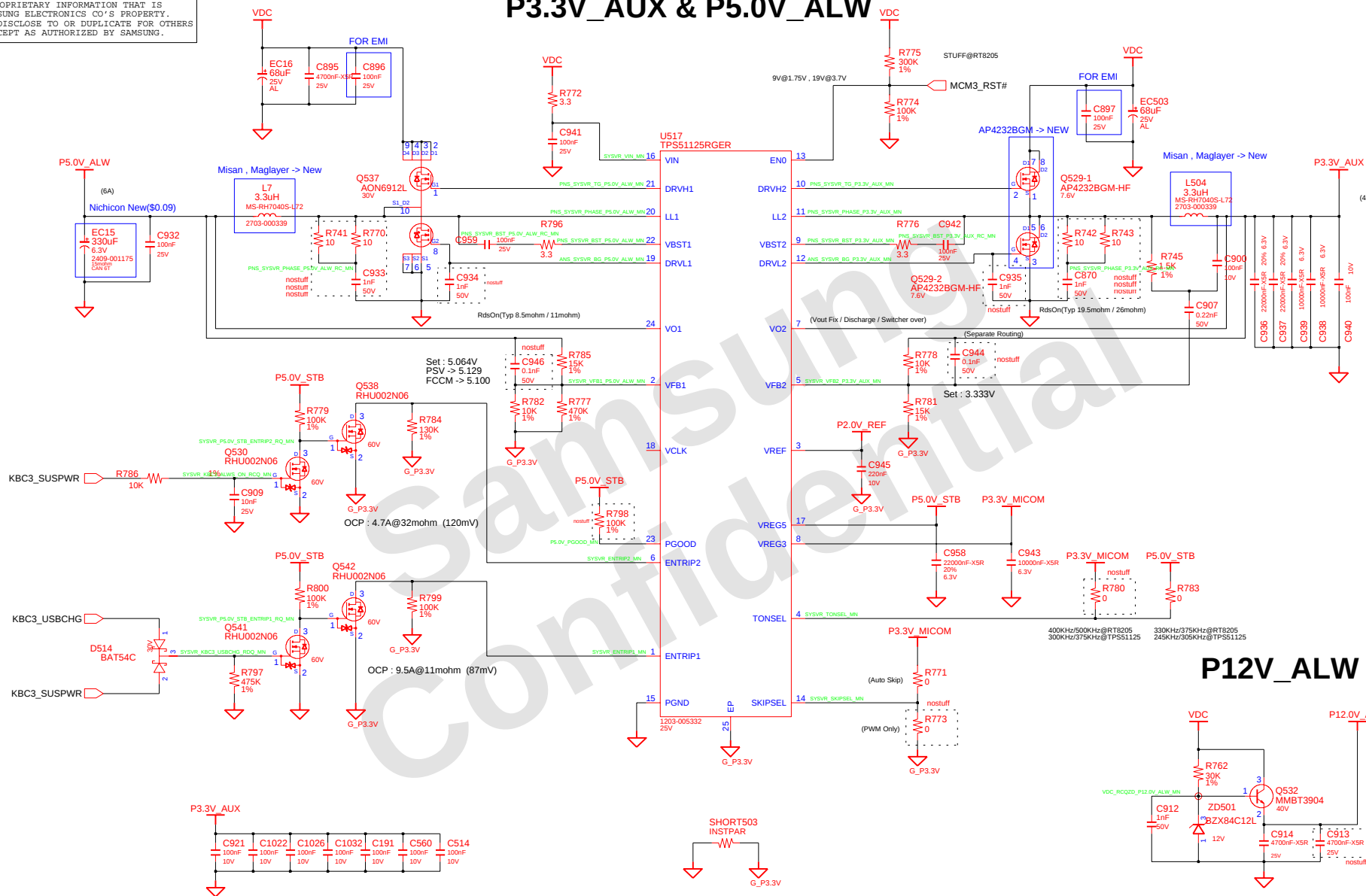
DRAW	Xiaohong Zhang	DATE	8/12/2006	TITLE	Suzhou_M	SAMSUNG
CHECK	Rujin Zheng	DEV. STEP	PV	LED_Switch		ELECTRONICS
APPROVAL	BC LEE	REV	1.0	LED_Switch		PART NO.
MODULE CODE		LAST EDIT	October 10, 2009 00:22:55 AM			BA41-01190/1/2A
				PAGE	50	OF 62

CHARGER & POWER MANAGEMENT



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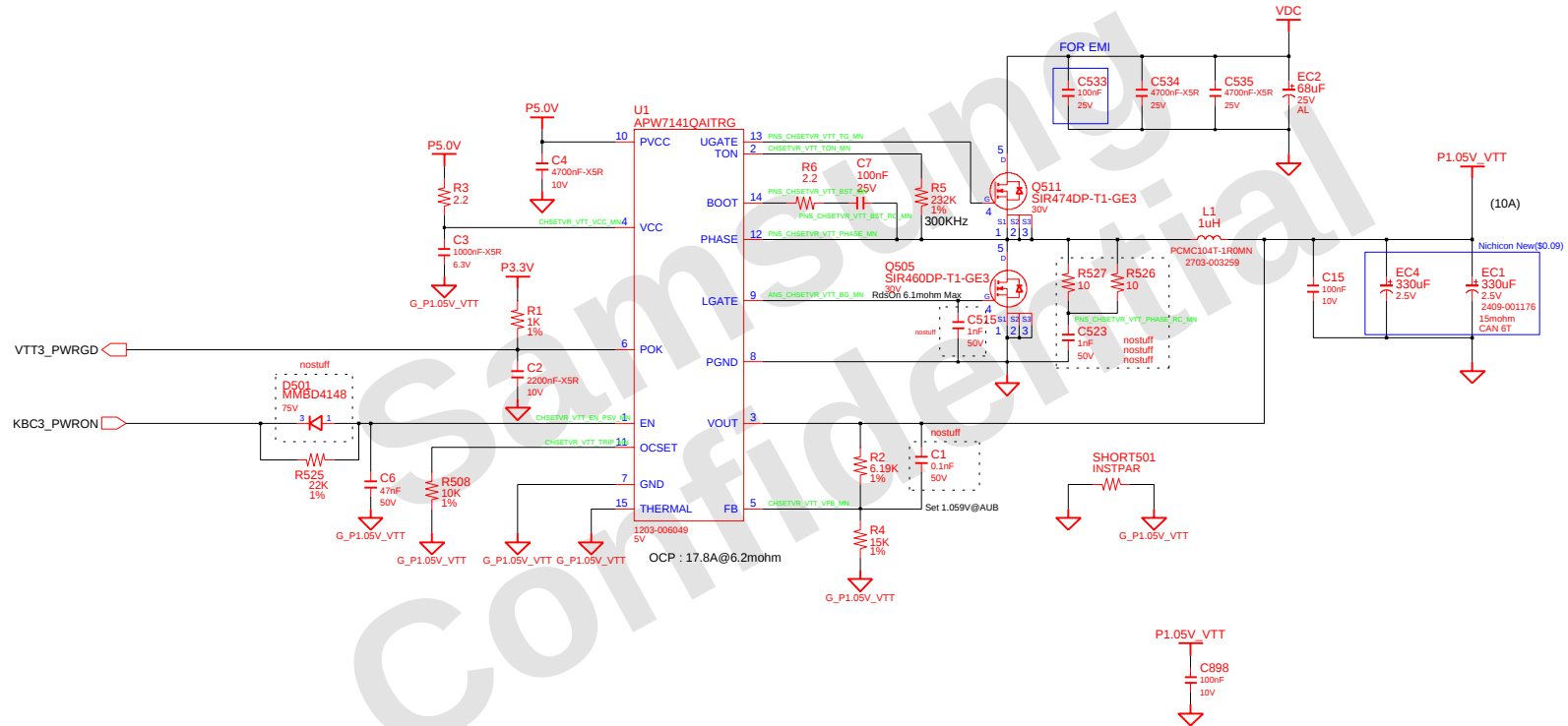
P3.3V_AUX & P5.0V_ALW



DRAW	Xiaohong Zhang	DATE	04/01/2009	Suzhou_M PWR_MV_3V_5V_R8205a P3.3V_AUX / P5.0V_AUX			
CHECK	Rujin Zheng	DEV. STEP	PV				
APPROVAL	BC LEE	REV	1.0		PART NO.	BA41-01190/1/2A	
MODULE CODE	undefined	LAST EDIT	October 10, 2009 00:22:55 AM		PAGE	52	OF 62

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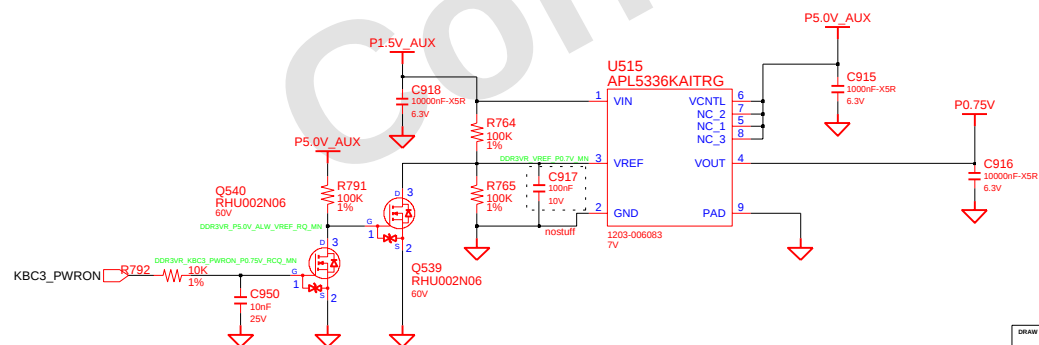
CHIPSET POWER(P1.05V_VTT & P1.05V)



DRAW	Xiaohong Zhang	DATE	03/11/2009	TITLE	Suzhou_M	SAMSUNG ELECTRONICS
CHECK	Rujin Zheng	DEV. STEP	PV		PWR_MV_Cantiga	
APPROVAL	BC LEE	REV	1.0		Chipset Power (P1.05V_M,P1.2V)	PART NO. BA41-01190/1/2A
MODULE CODE	undefined	LAST EDIT	October 10, 2009 00:22:55 AM	PAGE	53	OF 62

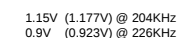
DDR3 Power

DDR3 VTT(0.75V)



COM-22C-015(1996.6.5) REV. 3

N10M-GE@13.36W



V _{ID1}	V _{ID0}	N11P-GE1	N11M-GE1
0	0		
0	1		
1	0	0.85V	0.85V
1	1	0.95V	1.03V

SHORT502
INSTPAR

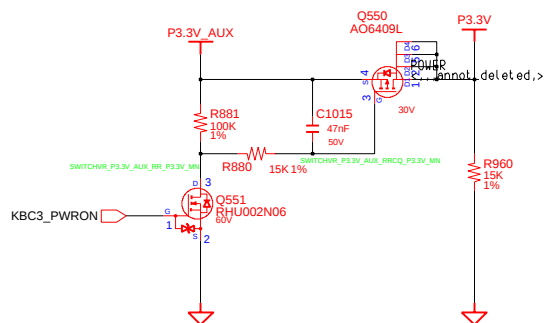


G EGF

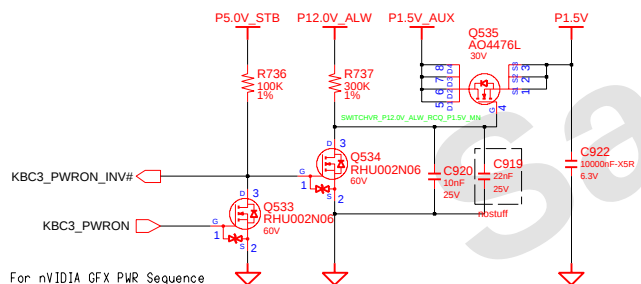
DRAW	Xiaohong Zhang	DATE	03/11/2009	TITLE	Suzhou_M	SAMSUNG ELECTRONICS		
CHECK	Rujin Zheng	REV. STEP	PV					
APPROVAL	BC LEE	REV	1.0					
MODULE CODE	LAST EDIT							
				Ext Gfx Memory(TPS51117)	PART NO.			BA41-01190/J12A
				October 10, 2009 00:22:55 AM	PAGE	56	OF	62

Switched Power

Switched Power On (P3.3V)



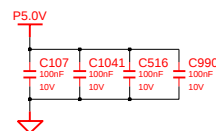
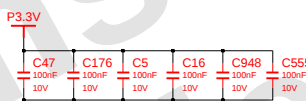
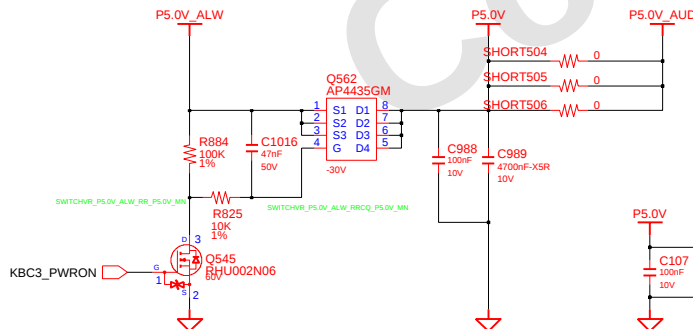
Switched Power On (P1.5V)



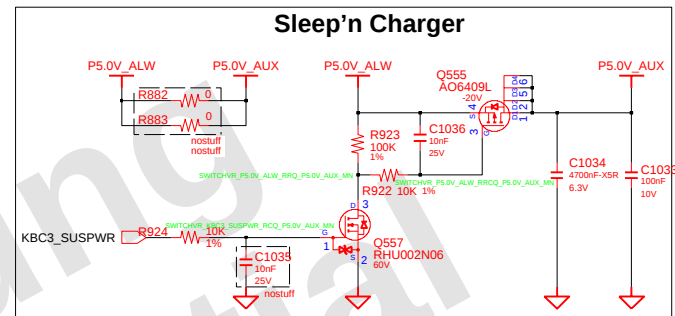
For nVIDIA GFX PWR Sequence

NVDD(EGFX_CORE) first and then FBVDD0(gDDR3)

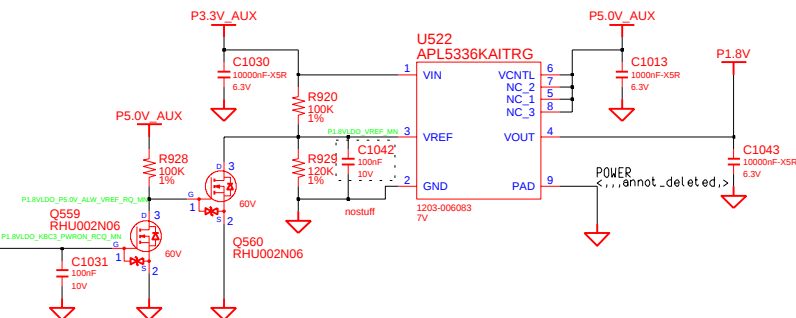
Switched Power On (P5.0V)



Sleep'n Charger

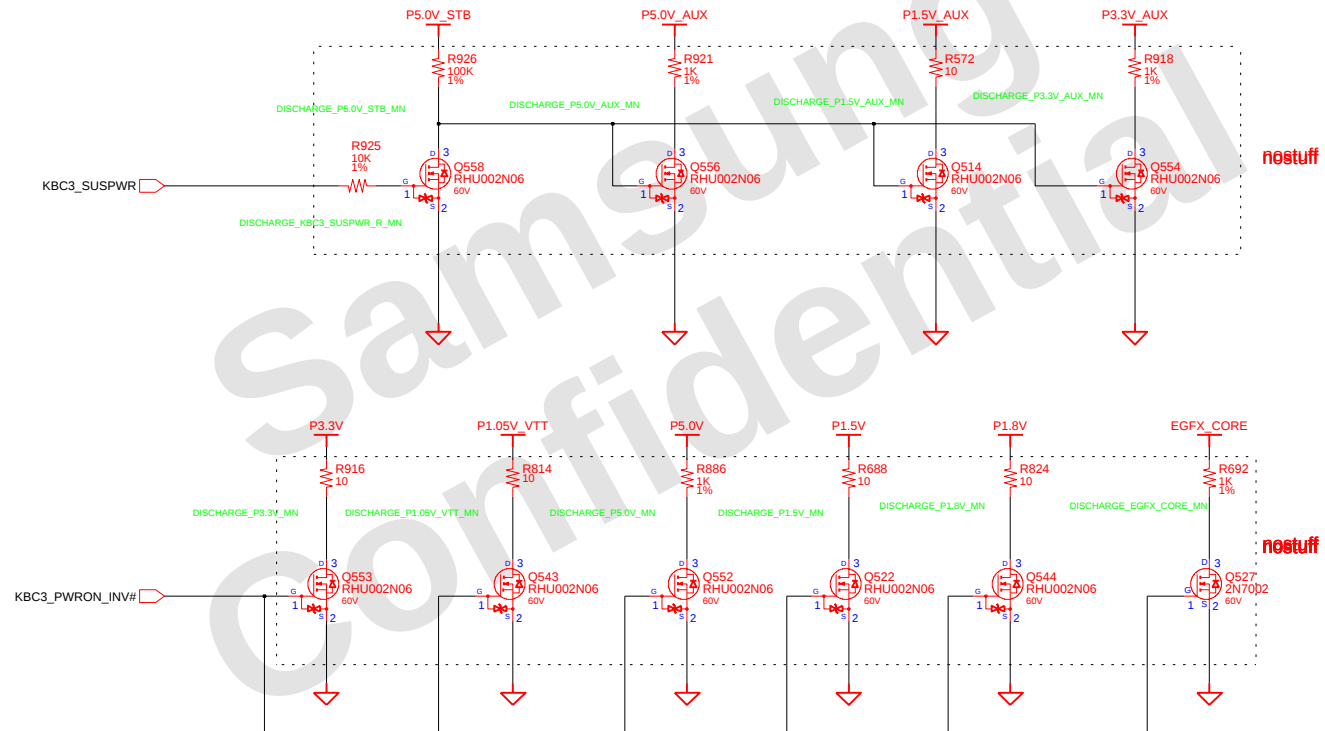


P1.8V(LDO)

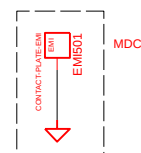
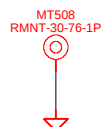
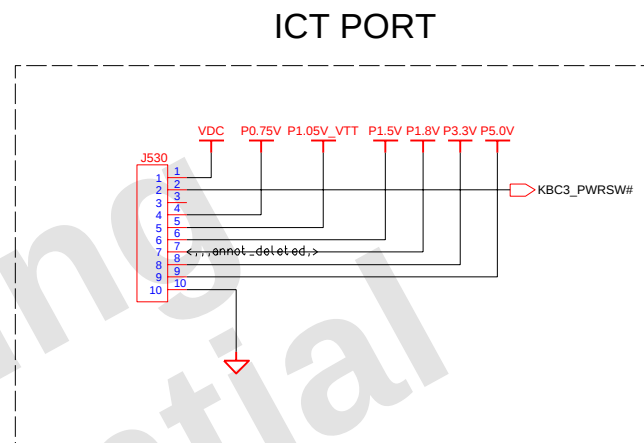


DRAW	Xiaohong Zhang	DATE	03/11/2009	TITLE	Suzhou_M	SAMSUNG ELECTRONICS
CHECK	Rujin Zheng	DEV. STEP	PV	PWR_MV_Switched		
APPROVAL	BC LEE	REV	1.0	SWITCHED POWER		
MODULE CODE		LAST EDIT				
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POWER DISCHARGER



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DRAW	Xiaohong Zhang	DATE	03/11/2009	TITLE	Suzhou_M		SAMSUNG ELECTRONICS			
CHECK	Rujin Zheng	REV. STEP	PV	PWR_MV_DisCharger		PART NO. BA41-01190/J2A				
APPROVAL	BC LEE	REV	1.0	DISCHARGING LOGIC						
MODULE CODE		undefined		LAST EDIT		October 10, 2009 00:22:55 AM	PAGE	59	OF	62

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- ☐ GPIO38
- ☐ AUD3_PD#
- ☐ FAN5_VDD
- ☐ SMB3_CLK
- ☐ SPI3_CLK
- ☐ SPI3_CS#
- ☐ ADT3_SEL#
- ☐ AUD3_SPKR
- ☐ CHP3_PECI
- ☐ CPU1_PSI#

- ☐ KBC3_A20G
- ☐ KBC3_VRON
- ☐ KBC5_TCLK
- ☐ LCD3_BRIT
- ☐ MCD3_SDWP
- ☐ MCM3_RST#
- ☐ PLT3_RST#
- ☐ SMB3_DATA
- ☐ SPI3_MISO
- ☐ SPI3_MOSI

- ☐ CLK3_CHP14
- ☐ CLK3_MMC48
- ☐ CRT3_GREEN
- ☐ CRT3_HSYNC
- ☐ CRT3_VSYNC
- ☐ KBC3_CHGEN
- ☐ KBC3_PWRGD
- ☐ KBC3_PWRON
- ☐ KBC3_RCIN#
- ☐ KBC5_TDATA
- ☐ MCD3_SDCD#
- ☐ MCD3_SDCCLK
- ☐ MCD3_SDCMD
- ☐ PEX3_WAKE#
- ☐ VTT3_PWRGD
- ☐ AUD5_CBN_MN
- ☐ AUD5_CBP_MN
- ☐ CHP3_PMSYNC

- ☐ CHP3_SERIRQ
- ☐ CHP3_SLPS3#
- ☐ CHP3_SLPS4#
- ☐ CHP3_SLPS5#
- ☐ CLK3_DBG LPC
- ☐ CLK3_PCI_FB
- ☐ CPU1_VID(0)
- ☐ CPU1_VID(1)
- ☐ CPU1_VID(2)
- ☐ CPU1_VID(3)
- ☐ CPU1_VID(4)
- ☐ CPU1_VID(5)
- ☐ CPU1_VID(6)
- ☐ CRT3_DDC CLK
- ☐ GFX3_ROM_SI
- ☐ GFX3_ROM_SO

GFX3_STRAP2

- ☐ KBC3_BKLTON
- ☐ KBC3_PWRSW#
- ☐ KBC3_RFOFF#
- ☐ KBC3_SMCLK#
- ☐ KBC3_SPI_DI
- ☐ KBC3_SPI_DO
- ☐ KBC3_SUSPWR
- ☐ KBC3_USBCHG
- ☐ KBC5_KSI(0)
- ☐ KBC5_KSI(1)
- ☐ KBC5_KSI(2)
- ☐ KBC5_KSI(3)
- ☐ KBC5_KSI(4)
- ☐ KBC5_KSI(5)
- ☐ KBC5_KSI(6)
- ☐ KBC5_KSI(7)
- ☐ KBC5_KSO(0)
- ☐ KBC5_KSO(1)

- ☐ KBC5_KSO(2)
- ☐ KBC5_KSO(3)
- ☐ KBC5_KSO(4)
- ☐ KBC5_KSO(5)
- ☐ KBC5_KSO(6)
- ☐ KBC5_KSO(7)
- ☐ KBC5_KSO(8)
- ☐ KBC5_KSO(9)

- ☐ LAN_RSET_MN
- ☐ LCD3_BKLTON
- ☐ LPC3_LAD(0)
- ☐ LPC3_LAD(1)
- ☐ LPC3_LAD(2)
- ☐ LPC3_LAD(3)
- ☐ MCD3_SDDAT0
- ☐ MCD3_SDDAT1
- ☐ MCD3_SDDAT2
- ☐ MCD3_SDDAT3
- ☐ PEG3_BKLTEN

- ☐SMB3_ALERT#
- ☐SPI0_WP#_MN
- ☐BAT3_DETECT#
- ☐CHP3_BATLOW#
- ☐CHP3_RTCRST#
- ☐CHP3_VREF_MN
- ☐CPU_TCK_R_MN
- ☐CRT3_DDCDATA

- ☐ EGFXVR_EN_MN
- ☐ EGFXVR_FB_MN
- ☐ EXP3_CLKREQ#
- ☐ FAN3_FDBACK#
- ☐ GFX3_THERMDN
- ☐ GFX3_THERMDP
- ☐ GFX3_VOLTID0
- ☐ GFX3_VOLTID1
- ☐ HDA3_AUD_SDO
- ☐ HDA3_BCLK_MN
- ☐ HDA3_MDC_SDO

- ☐ KBC3_BATDET#
- ☐ KBC3_CHG4.2V
- ☐ KBC3_EXTSMI#
- ☐ KBC3_PWRBTN#
- ☐ KBC3_RSMRST#
- ☐ KBC3_RUNSCI#
- ☐ KBC3_SMDATA#
- ☐ KBC3_SPI_CLK
- ☐ KBC3_SPI_CS#

- ☐ KBC3_TX_J_MN
- ☐ KBC5_KSO(10)
- ☐ KBC5_KSO(11)
- ☐ KBC5_KSO(12)
- ☐ KBC5_KSO(13)
- ☐ KBC5_KSO(14)
- ☐ KBC5_KSO(15)
- ☐ KBC5_USBCHG#
- ☐ LAN3_CLKREQ#

- ☐ LID3_SWITCH#
- ☐ LPC3_LFRAME#
- ☐ MEM3_CHB_SA0
- ☐ MEM3_CHB_SA1
- ☐ MIN3_CLKREQ#
- ☐ PCH_GPIO0_MN
- ☐ PC13_CLKRUN#

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AUD5_CPVEE_MN
AUD5_SENS_HP#
CHP3_SATALED#
CHP3_SUSSTAT#
CPU0_COMP0_MN
CPU0_COMP1_MN
CPU0_COMP2_MN
CPU0_COMP3_MN
CPU1_DPRSLPVR
CPU1_VCCSENSE
CPU1_VSSSENSE
CPUVR_CS_N1_MN
CPUVR_CS_N2_MN
CPUVR_CS_P1_MN
CPUVR_CS_P2_MN
DDR3VR_TON_MN
GFX1_VDDSENSE
GFX3_ROM_SCLCK
HDA3_AUD_BCLK
HDA3_AUD_RST#
HDA3_AUD_SDIO
HDA3_AUD_SYNC
HDA3_MDC_BCLK
HDA3_MDC_RST#
HDA3_MDC_SD1
HDA3_MDC_SYNC
KBC3_CAPSLED#
KBC3_SPMUTER
KBC3_WAKESC#
KBC5_LED_CTRL
LDC3_EDID_CLK
MCP1_DRAMRST#
PCH_GPIO36_MN
PCH_GPIO48_MN
PCI3_IRDY#_MN
PCI3_PERR#_MN
PCI3_REQ1#_MN
PCI3_REQ2#_MN
PEGO_ZQ_R1_MN
PEGO_ZQ_R2_MN
PEGO_ZQ_R3_MN
PEGO_ZQ_R4_MN
PEGO_ZQ_R5_MN
PEGO_ZQ_R7_MN
VGAS_HDMI_HPD
AUD0_CPVREF_MN
AUD5_HP_O_LEFT
AUD5_MIC2_VREF
AUD5_SENS_A_MN
AUD5_SENS_MIC#
CHP3_CPU_PWRGD
CHP3_GPIO39_MN
CHP3_INTRUDER#
CLK3_PCLXMMCOM
CLOCK_P15V_MN
CLOCK_P33V_MN
CPU1_THRMTRIP#
PEG3_HDMI_CLK
PEG3_HPD_HDMI
PEG3_LCDVDDON
PEG3_SPOIF_MN
PEG3_VDD33_MN
PEG5_HDMI_CLK
PLT3_RST_ORG#
SPI3_HOLD#_MN
TP_LED3_R1_MN
TP_LED3_R2_MN
TP_LED3_R3_MN
TP_LED3_R4_MN
TP_LED3_R5_MN
TP_LED3_R6_MN
TP_LED3_R7_MN
TP_LED3_R8_MN
TP_LED3_R9_MN
CPUVR_DR0OP_MN
CPUVR_THERM_MN
CPU_CFG_7_R_MN
DDR3VR_TRIP_MN
EGFXVR_D1_R_MN
EGFXVR_ILUM_MN
EGFXVR_VOUT_MN
KBC3_LED_ACIN#
KBC3_USBPWRON#
KBC3_WLON_LED#
LDC3_EDID_DATA
PC13_FRAME#_MN
PC13_PIRQA#_MN
PC13_PIRQB#_MN
PC13_PIRQC#_MN
PC13_PIRQD#_MN
PEG1_PLLVDD_MN
PEG3_HDMI_DATA
PEG5_HDMI_DATA
THM3_STP#_Q_MN
THM3_STP#_R_MN
TPDS_L_BUTTON#
TPDS_R_BUTTON#
TP_LED3_R10_MN
TP_LED3_R11_MN
TP_LED3_R12_MN
TP_LED3_R13_MN
TP_LED3_R14_MN
TP_LED3_R15_MN
TP_LED3_R16_MN
TP_LED3_R17_MN
TP_LED3_R18_MN
VRM3_CPU_PWRGD
VRM3_IMVP_IMON
ANS_CHGVR_BG_MN
ANS_HP_O_RIGHT
AUD5_JREF_R_MN
CHP1_DRAM_PWRGD
CHP3_ME_RTCRST#
CHP3_SUSPWR_ACK
CHP3_WPI#_O_R_MN
CPUVR_VSFILT_MN
DDR3VR_PGOOD_MN
KBC3_LED_POWER#
KBC3_PWRGD_R_MN
KBC3_PWRON_INV#
MDC48_TIP_B1_MN
MDC48_TIP_B2_MN
MEM3_CHA_SA0_MN
MEM3_CHA_SA1_MN
PCH_PCIECLKRQ2#
PNS_CHGVR_TG_MN
SUB_KBC3_PWRSW#
SYSVR_TONSEL_MN
THM3_DP2_DP3_MN
THM3_DP2_DP3_MN
VRM3_CLK_PWRGD#
VTT3_PWRGD_R_MN
ANS_CPUVR_BG1_MN
ANS_CPUVR_BG2_MN
ANS_DDR3VR_BG_MN
ANS_EGFXVR_BG_MN
CHP3_VREF_SUS_MN
CLOCK_CPU_SEL_MN
CLOCK_XTAL_IN_MN
CPUVR_CSP1_RC_MN
CPUVR_CSP2_RC_MN
CPUVR_TRIPSEL_MN
DDR3VR_EN_PSV_MN
HDD3_LED#_LED_MN
KBC3_LED_CHARGE#
KBC3_THERM_SMCLK
MDC48_RING_B1_MN
MDC48_RING_B2_MN
PEG0_BURST#_N_MN
PEG3_DACA_VDD_MN
PEG3_TESTMODE_MN
PEG3_XTAL_OUT_MN
PLT1_RST#_MCP_MN
PNS_CPUVR_TG1_MN
PNS_CPUVR_TG2_MN
PNS_DDR3VR_TG_MN
PNS_EGFXVR_TG_MN
SYSVR_ENTRIP1_MN
SYSVR_ENTRIP2_MN
SYSVR_SKIPSEL_MN
THM3_SHDN_SEL_MN
THM3_TRIP_SET_MN
AUD5_HP_LEFT_B_MN
AUD5_HP_LEFT_R_MN
CLK3_MMC48_PCH_MN
CLOCK_CPU_STOP#_MN
CLOCK_XTAL_OUT_MN
LAN3_CLKREQ#_R_MN
MCH1_SM_RCOMP0_MN
MCH1_SM_RCOMP1_MN
MCH1_SM_RCOMP2_MN
MCP3_PEG_RBIAS_MN
PEG1_FBA_DEBUG_MN
PEG1_FBC_DEBUG_MN
PEG1_IFPEF_PLLVDD
PEG1_PB_LLAVDD_MN
PEG1_SP_PLLVDD_MN
PNS_CPUVR_BST1_MN
PNS_DDR3VR_BST_MN
PNS_EGFXVR_BST_MN
PRTC_BAT_CON_R_MN
SYS3_LED_POWER_MN
808H_CHP3_SERIRQ_MN
AUD5_HP_RIGHT_B_MN
AUD5_MIC2_INT_B_MN
AUD5_MIC2_INT_J_MN
CHGVR_SGATE_RRQ_MN
CHP1_DRAM_PWRGF_MN
CHP3_PEG_HOLD_RST#
CHP3_XTAL_IN_Z5_MN
CHSETVR_VTT_TON_MN
CHSETVR_VTT_VCC_MN
CHSETVR_VTT_VFB_MN
CLK3_DBFLPC_PCH_MN
CLK3_PCL_FB_PCH_MN
EGFXVR_D0_D1_RC_MN
HDA3_MDC_SD1L_R_MN
KBC5_LED_CTRL_R_MN
LAN3_DISABLE#_R_MN
P15V_VREFCA_R1_MN
P15V_VREFCA_R2_MN
P15V_VREFCA_R3_MN
P15V_VREFCA_R4_MN
P15V_VREFCA_R5_MN
P15V_VREFCA_R6_MN
P15V_VREFCA_R7_MN
P15V_VREFCA_R8_MN
P15V_VREFCA_R9_MN
P15V_VREFDQ_R1_MN
P15V_VREFDQ_R2_MN
P15V_VREFDQ_R3_MN
P15V_VREFDQ_R4_MN
P15V_VREFDQ_R5_MN
P15V_VREFDQ_R6_MN
P15V_VREFDQ_R8_MN
PEG5_HDMI_CLK_B_MN
PEG1_IFPC_PLLVDD_MN
VGAS_HDMI_HPD_R_MN
AUD5_MIC1_LEFT_C_MN
AUD5_MIC1_LEFT_J_MN
AUD5_MIC1_LEFT_R_MN
AUD5_MIC2_LEFT_C_MN
CHP3_XTAL_OUT_Z5_MN
CHSETVR_VTT_TRIP_MN
KBC5_LED_CTRL_QC_MN
KBC5_LED_CTRL_QR_MN
PEG1_IFPAB_IOVDD_MN
PEG1_IFPEF_IOVDD_MN
PEG3_JTAG_TRST_N_MN

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○PNS_CPUVR_PHASE1_MN
○PNS_CPUVR_PHASE2_MN
○PNS_DDR3VR_PHASE_MN
○PNS_EGFXVR_PHASE_MN
○VIM3_CLK_PWRGD0_INV
○AUD5_MIC1_RIGHT_C_MN
○AUD5_MIC1_RIGHT_I_MN
○AUD5_MIC1_RIGHT_R_MN
○AUD5_MIC1_VREF0_I_MN
○AUD5_MIC2_RIGHT_C_MN
○CHP1_SATAICOMP0IO_MN

○DDR3VR_VREF_P0.7V_MN
○KBC3_CAPSLED0_LED_MN
○MCP3_FDI_SIDE0AND_MN

○PEG3_PEX_SVDD_SVS_MN
○PEG3_TX_HDMI_PD_Q_MN
○PEG3_XTAL_OUTBUFF_MN
○PNS_CPUVR_BST1_RC_MN

○PNS_DDR3VR_BST_RC_MN
○PNS_EGFXVR_BST_RC_MN
○ANS_CHSETVR_VTT_BG_MN
○CHSETVR_VTT_EN_PSV_MN

○CPU1_THRMTRIP#_PCH_MN

○KBC3_WLON_LED#_LED_MN
○MCP3_PEG_IR_COMP0IO_MN
○PCH_DM1_P1.05V_VTT_MN

○PEG3_LCD3_EDID_CLK_MN

○PEX1_EXPCRD_TXN3_C_MN
○PEX1_EXPCRD_TXP3_C_MN
○PNS_CHSETVR_VTT_TG_MN
○P5.0V_AUX_USBPWR_P2_MN

○PEG3_LCD3_EDID_DATA_MN
○PNS_CHSETVR_VTT_BST_MN
○PNS_CPUVR_PHASE1_RC_MN
○PNS_CPUVR_PHASE2_RC_MN
○PNS_DDR3VR_PHASE1_RC_MN
○CLK3_MICOM_32K_XTAL1_MN
○CLK3_MICOM_32K_XTAL2_MN

○SYSVR_VFB1_P5.0V_ALW_MN
○SYSVR_VFB2_P3.3V_AUX_MN

○PNS_CHSETVR_VTT_PHASE_MN
○SYSVR_KBC3_USBCHG_RDQ_MN

○SYSVR_VOUT2_P3.3V_AUX_MN
○ANS_SYSVR_BG_P3.3V_AUX_MN
○ANS_SYSVR_BG_P5.0V_ALW_MN

○PNS_CHSETVR_VTT_BST_RC_MN
○PNS_SYSVR_TG_P3.3V_AUX_MN
○PNS_SYSVR_TG_P5.0V_ALW_MN
○SYSVR_KBC3_ALWS_ON_RCQ_MN
○P1.8VDDO_KBC3_PWRON_RCQ_MN
○PNS_SYSVR_BST_P3.3V_AUX_MN
○PNS_SYSVR_BST_P5.0V_ALW_MN

○DDR3VR_P5.0V_ALW_VREF_RQ_MN
○PNS_CHSETVR_VTT_PHASE_RC_MN

○PNS_SYSVR_PHASE_P3.3V_AUX_MN
○PNS_SYSVR_PHASE_P5.0V_ALW_MN
○P1.8VDDO_P5.0V_ALW_VREF_RQ_MN
○PNS_SYSVR_BST_P3.3V_AUX_RC_MN
○PNS_SYSVR_BST_P5.0V_ALW_RC_MN
○SYSVR_P5.0V_STB_ENTRIP1_RQ_MN
○SYSVR_P5.0V_STB_ENTRIP2_RQ_MN
○SWTCHVR_P5.0V_ALW_RR_P5.0V_MN
○DDR3VR_KBC3_PWRON_P0.75V_RCQ_MN
○PNS_SYSVR_PHASE_P3.3V_AUX_RC_MN
○PNS_SYSVR_PHASE_P5.0V_ALW_RC_MN
○SWTCHVR_P3.3V_AUX_RRCQ_P3.3V_MN
○SWTCHVR_P5.0V_ALW_RRCQ_P5.0V_AUX_MN

○SWTCHVR_KBC3_SUSPWR_RCQ_P5.0V_AUX_MN

○BGATE
○CPU_CORE
○CPU_CORE
○CPU_CORE
○EGFX_CORE
○EGFX_CORE
○EGFX_CORE
○G_AUD
○G_AUD
○G_CHG
○G_CHG
○G_CPU

○G_DDR
○G_DDR
○G_EGFX
○G_EGFX
○G_P3.3V
○G_P3.3V
○G_P1.05V_VTT
○G_P1.05V_VTT
○LCD_VDD3V
○LCD_VDD3V
○MDC_GND
○MDC_GND
○P1.5V
○P1.5V
○P1.5V
○P1.8V
○P1.8V
○P1.8V
○P3.3V
○P3.3V
○P3.3V
○P5.0V
○P5.0V
○P5.0V
○P0.75V
○P0.75V
○P1.0V_LAN
○P1.0V_LAN
○P1.5V_AUX
○P1.5V_AUX

○P1.8V_LAN
○P2.0V_REF

○P5.0V_ALW
○P5.0V_ALW
○P5.0V_AUD
○P5.0V_AUD
○P5.0V_AUX
○P5.0V_AUX
○P5.0V_STB
○P5.0V_STB
○P1.05V_VTT
○P1.05V_VTT
○P1.05V_VTT
○P1.05V_VTT

○P12.0V_ALW
○P12.0V_ALW
○P4.75V_AUD
○P4.75V_AUD
○P2.39V_VREF

○P3.3V_MICOM
○P3.3V_MICOM
○SUB_GND
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○SUB_P3.3V
○SUB_P3.3V
○SUB_P5.0V_AUX
○SUB_P5.0V_AUX
○VDC
○VDC
○VDC
○VDC
○VCC_CRT
○VCC_CRT
○VCC_LED
○VCC_LED
○VDC_ADPT
○VDC_ADPT